SPECTROSCOPIC QUANTUM IMAGING USING PIXEL-LEVEL ADCS IN SEMICONDUCTOR-BASED HYBRID PIXEL DETECTORS

David San Segundo Bello

Samenstelling promotiecommissie:

Voorzitter:	prof.dr.ir. A.J. Mouthaan	
Secretaris:	prof.dr.ir. A.J. Mouthaan	Universiteit Twente, EWI
Promotor:	prof.dr.ir. B.Nauta	Universiteit Twente, EWI
Ass. promotor:	dr. J.L. Visschers	NIKHEF
Referent:	dr. E. Heijne	CERN
Leden:	prof.dr. J. Schmitz	Universiteit Twente, EWI
	prof.dr.ir. G.J.M. Smit	Universiteit Twente, EWI
	prof.dr.ir. A.J.P. Theuwissen	TU Delft

Title:	SPECTROSCOPIC QUANTUM IMAGING USING PIXEL-LEVEL ADCS IN SEMICONDUCTOR-BASED HYBRID PIXEL DETECTORS
Author:	David San Segundo Bello
ISBN:	978-90-365-2852-8
DOI:	10.3990./1.9789036528528

This research was partially supported by the European Union under the Grant number TMR ERBFMRXCT980196

SPECTROSCOPIC QUANTUM IMAGING USING PIXEL-LEVEL ADCS IN SEMICONDUCTOR-BASED HYBRID PIXEL DETECTORS

Proefschrift

ter verkrijging van
de graad van doctor aan de Universiteit Twente,
op gezag van de Rector Magnificus,
Prof.dr. H. Brinksma,
volgens besluit van het College voor Promoties
in het openbaar te verdedigen
op donderdag 10 september 2009 om 15.00 uur

door

David San Segundo Bello

geboren op 21 augustus 1972
te Hospitalet de Llobregat, Spanje

Dit proefschrift is goedgekeurd door:

de promotor prof.dr.ir. B. Nauta
de assistent promotor dr. J. Visschers

Para David, Inés y Merche.

Contents

List of Figures

List of Tables

Samenvatting

In algemeen gebruikte radiografische beeldopnemers is de waarde gemeten voor iedere pixel gelijk aan de totale lading gegenereerd door de energie geabsorbeerd tijdens de volledige integratietijd, met een bepaalde efficiëntie lager dan 100 procent. Deze efficiëntie is afhankelijk van de invallende stralingsenergie. Lading kan tijdens de belichtingsperiode ook opgewekt worden als gevolg van fysische processen die de ruis in de gemeten hoeveelheid verhogen, en hiermee de beeldkwaliteit verlagen.

Hoofdstuk 2 geeft een overzicht van de kenmerken van Röntgenstraling en gammastraling, hoe deze ontstaan, hoe ze interageren met materie, en welke technieken gebruikt kunnen worden om ze te detecteren.

Hoofdstuk 3 biedt een inleiding tot stralingsdetectoren gebaseerd op halfgeleidertechnologie. Dit hoofdstuk verklaart het proces van het ontstaan van lading en het accumuleren van lading in detectoren gebaseerd op halfgeleidermaterialen, en presenteert de meest belangrijke positiegevoelige detectoren gebaseerd op halfgeleiders. Hybride pixel detectoren voor photon quantification worden ook besproken in dit hoofdstuk, als erkenning dat deze thesis een voortzetting is van de research in dit onderzoeksgebied tijdens de voorbij jaren.

Een beeld gebaseerd op de accumulatie van lading gegenereerd door alle invallende fotonen is niet altijd de meest optimale oplossing. Bijvoorbeeld, bij transmissie radiografie hebben sommige van de door de bron uitgestraalde fotonen een hoge energie, en worden bijna nooit geabsorbeerd door het bestraalde object. Terwijl deze fotonen weinig tot geen nuttige informatie bijdragen, nemen ze wel een buitenproportionele fractie van het signaal in. Daarentegen is de passage van een laag-energie foton doorheen het subject minder waarschijnlijk, terwijl deze meer nuttige informatie met zich meebrengt, maar slechts een relatief klein signaal in de detector opwekt. Om de beeldkwaliteit te verhogen dienen fotonen met lagere energieniveaus een hoger gewicht te krijgen.

Deze thesis beschrijft eerst de elektronica die de door het foton opgewekte lading verwerkt, voor de analoog-digitaal conversie. De gebruikte circuits zijn welbekend in het domein en zijn zeer gelijkaardig aan de circuits gebruikt in de Medipix2 uitleeschip. De enige nieuwigheid hier is het gebruik van afzonderlijke voedingen voor het analoge signaalverwerkingsgedeelte (de ladingsgevoelige versterker en het peak-and-hold circuit) en voor de hit detection circuits. De uitgang van het hit detection circuit is een digitaal signaal dat gebruikt zal worden in zowel het digitale gedeelte van de ADC als in het digitale uitleescircuit. Zo kan zowel in het hit detection circuit als in alle andere digitale circuits een lagere voedingsspanning gebruikt worden, teneinde het vermogenverbruik in de pixels te verlagen.

Hoofdstuk 4 geeft een overzicht van het volledige systeem beschreven in

deze thesis. Aan het begin van dit hoofdstuk wordt aangetoond dat het gebruik van analoog-digitaal converters (ADCs) op pixel niveau de beste methode is om een pixel detector uitlees chip te ontwerpen voor spectroscopische beeldvorming. Vervolgens worden de verschillende componenten van het systeem voorgesteld om een algemeen idee te krijgen van de werking van het systeem. De volgende hoofdstukken beschrijven elke component in detail.

In **hoofdstuk 5** wordt het ontwerp van de front-end circuits die het detector signaal verwerken voor de analoog-digitaal conversie behandeld. Eerst wordt de ingangsversterker besproken die de detector stroom integreert. De tweede component is de hit detector, die de inslag van een foton op de pixel aan de andere componenten signaleert. De laatste component die aan bod komt in dit hoofdstuk is het circuit dat het resultaat van de stroomintegratie bijhoudt voor conversie door de ADC.

Hoofdstuk 6 beschrijft het ontwerp van de ADCs gesitueerd in de pixels. Twee types van ADCs worden onderzocht: een successive approximation ADC en een algoritmische ADC. Het ontwerp van elke ADC is beschreven, evenals metingen op prototypes. Het gebruik van ADCs op pixel niveau in quantum beeldopnemers is een eerste nieuwigheid gentroduceerd in deze thesis. Deze ADCs moeten geplaatst worden in elke pixel van de uitleeschip, en functioneren onafhankelijk van elkaar.

De tweede nieuwigheid is de asynchrone, event-driven uitleestopologie van de pixels in de matrix. Elke foton interactie wordt verwerkt en uitgelezen van de pixel (onafhankelijk), en de uitleessequentie wordt gestart door de pixels. In **hoofdstuk 7** wordt de gebruikte topologie om de data van de pixels te lezen (de uitgang van de ADC en het adres van de pixel) besproken, evenals het selecteren van de uit te lezen pixel. Het selecteren van de pixel is gebaseerd op een double-column token ring topologie, en de pixel data wordt gelezen door middel van current-mode signaling.

Het werk voorgesteld in deze thesis toont aan dat complexe signaalverwerking op pixel niveau mogelijk is in quantum beeldopnemers gebaseerd op hybride pixel detectoren. Niettemin zou het systeem beschreven in deze thesis uitgebreid kunnen worden zonder deze topologie te verliezen. Bijvoorbeeld, door informatie toe te voegen betreffende het tijdstip waarop het foton de pixel raakt. Of door de digitale signaalverwerking in de pixels uit te breiden om bijvoorbeeld rekening te houden met meerdere fotonen die de pixel raken op hetzelfde tijdstip.

Chapter 1

Introduction

1.1 Background and motivation

Within a few months of the discovery of X-rays by Wilhelm Conrad Röntgen at the end of 1895, radiography was born and laboratories and hospitals all over Europe and the U.S.A. were devising applications for the newly discovered radiation [1]. In 1900, Paul Villard discovered gamma-rays. They were considered to be different from X-rays because they had a much greater penetrating depth. Gamma-rays were emitted from radioactive substances and, like X-rays, were not affected by electric or magnetic fields. It wasn't until 1914 that Rutherford showed that gamma-rays were, like X-rays, a form of electromagnetic radiation but with a shorter wavelength (or higher energy) than X-rays.

Since their discovery, the number of applications for X-rays and gamma-rays has continually increased, and nowadays X-rays and gamma-rays are used in countless applications in medicine, biology, material analysis, astronomy, etc.

In commonly-used radiographic imaging devices, the quantity measured for each pixel is the total charge generated by the energy absorbed in the detector during the total exposure time, with some efficiency less than 100 percent. This efficiency depends on the energy of the incident radiation. Also, charge can be generated during the exposure time due to natural processes which increase the noise in the measured quantity, degrading the quality of the image.

Having an image based on the accumulation of the charge generated by all arriving photons is not always the optimal solution. For example, in transmission radiography some of the photons emitted by the source have a high energy and are almost never absorbed by the subject. While these photons contribute essentially little or no useful information, they contribute a disproportionate fraction of the signal. In contrast, the passage of a lower energy photon through the subject is less likely, but often provides more information, while at the same time it generates a relatively small signal in the detector. To improve the quality of the final image, the photons having energy levels that cause them to be more attenuated should be weighted with larger values.

In most detector materials the charge generated after a photon interaction is proportional to the energy lost by the photon. In the case of semiconductor materials this proportionality is linear over a wide range of photon energies. If this charge is measured for each individual photon interaction, and not accu-

mulated during the total exposure time, a more accurate measurement of the energy absorbed in the detector can be obtained, leading to better radiographic images. This is the principle behind *quantum imaging systems*, so called because they can detect individual quanta (photons in this case).

The simplest quantum imaging systems use *photon counting* to create the final radiographic image. In a photon counting imaging system, a comparison is made between the signal from the sensor and a threshold. If the signal is above the threshold, it is considered to correspond to a photon interaction and the contents of a counter are increased. The net result is that, irrespective of the energy carried by the photon, each interaction is given the same weight in the final image. However, taking into consideration the proportionality of the signal from the sensor to the photon energy can lead to many more imaging possibilities [2].

1.2 Overview of the achievements

This thesis describes the design of a microelectronic system that can be used to build a spectroscopic imaging system, in particular a *spectroscopic quantum imaging using pixel-level ADCs in semiconductor-based hybrid pixel detectors*. In such a system the signal generated in the sensor by a photon interaction is electronically processed to obtain a measurement of the energy deposited by the photon. This measurement is expressed as a digital value and read from the pixel by the appropriate circuitry located in the periphery of the chip. The digital data corresponding to the measurement (energy of the photon and pixel address in the imaging array) is then read from the chip by an external data acquisition system for further processing or visual presentation.

This work describes a feasibility study for the use of pixel level ADCs in quantum imaging systems. As such, it is not targeted for a specific application, and the specifications that will be derived aim to cover a wide range of possibilities. For each specific application different optimizations can be made and we will mention these optimizations in the text where applicable. The aim of this work is the design of a pixel detector readout chip connected to semiconductor-based detectors, although the same principle can be used for other types of detectors.

Two different pixel-level ADCs have been designed and measured which have the characteristics needed to be used in such a spectroscopic quantum imaging system. These ADCs have been designed with no specific application target in mind, and thus the specifications used might not fit all applications. Nevertheless, the chosen architectures can be scaled in terms of resolution or conversion speed without large increases in occupied area or dissipated power. A readout architecture has also been designed to be used in such an imaging system, where each pixel essentially works as an independent system in itself. The architecture allows different configurations for different optimizations.

For the purpose of verifying the functionality of the different blocks, several chips have been designed, manufactured and tested. All the prototype chips designed and tested during the length of this work were fabricated in the same CMOS 0.25μm technology. This technology allows up to six layers of metal interconnect but, with the exception of the first prototype chip, all chips were designed and fabricated with only three layers of metal interconnect due to

limitations of the multi-project wafer (MPW) runs*. All circuits were designed full-custom, with the exception of the input and output pads, which were taken from the library designed at CERN for this technology.

The first prototype chip, called pixADC1, was sent for fabrication in the same reticle as the Medipix2 readout chip [3] in December 2000. Figures 1.1 and 1.2 show, respectively, the layout and a photograph of the chip. This chip occupies an area of 1 mm by 3.6 mm. The pixADC1 chip contains three different designs for pixel-level ADCs as well as the array of current sources used in the DACs discussed in [4].

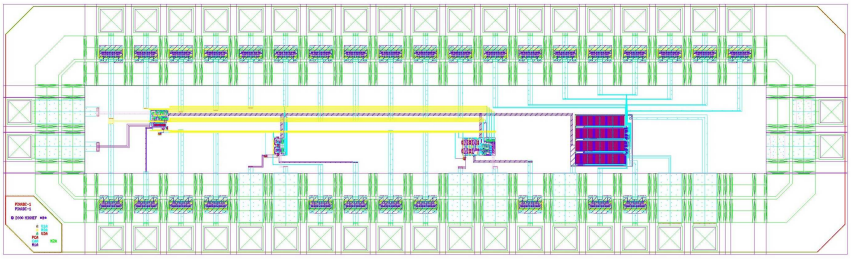

Figure 1.1: Layout of the pixADC1 prototype chip.

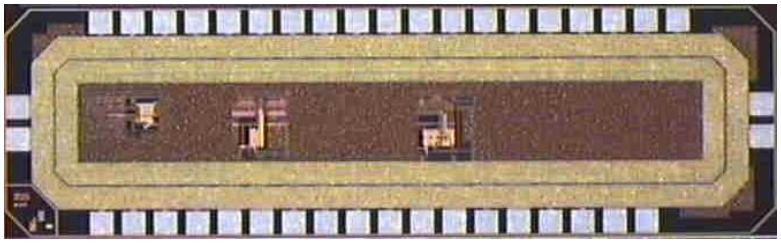

Figure 1.2: Photograph of the pixADC1 prototype chip.

A second prototype chip (pixADC2) was sent for fabrication in November 2001 as part of a multi-project wafer (MPW). Figures 1.3 and 1.4 show, respectively, the layout and a photograph of the chip. This chip has a size of 2 mm by 2 mm and it contains the designs for pixel-level ADCs where the problems found during the testing of pixADC1 were solved. The successive approximation ADC has an area of 105 μm by 85 μm, and the algorithmic ADC an area of 99 μm by 56 μm.

A third prototype chip (pixADC3) was sent for fabrication in April 2002 as part of a multi-project wafer. Figure 1.5 shows the layout of the chip, and figure 1.6 shows a photograph of the chip. The chip has a size of 2 mm by 4 mm and contains an array of 8 by 8 successive approximation ADCs. These

*The MPW service was organized by the Microelectronics department of the European Center for Particle Physics (CERN) in Geneva, Switzerland.

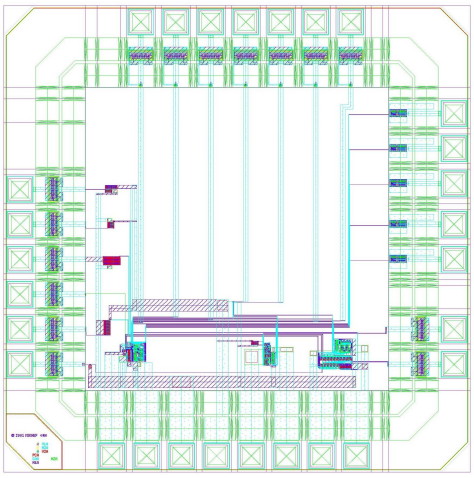

Figure 1.3: Layout of the pixADC2 prototype chip.

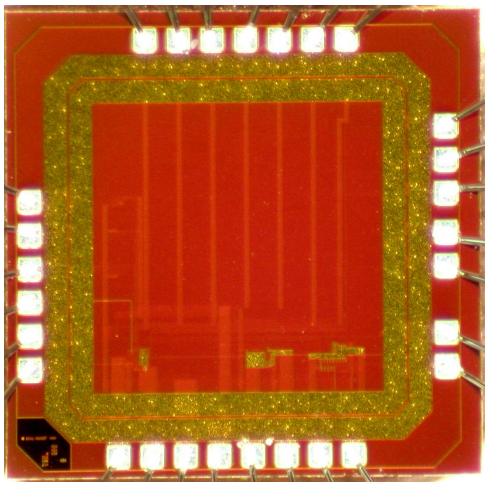

Figure 1.4: Photograph of the pixADC2 prototype chip.

ADCs are designed like the ones found in the pixADC2 prototype chip but the layout is optimized to occupy only 85 by 85 μm. It is used to test the digital data readout from the ADCs as well as the uniformity of their response.

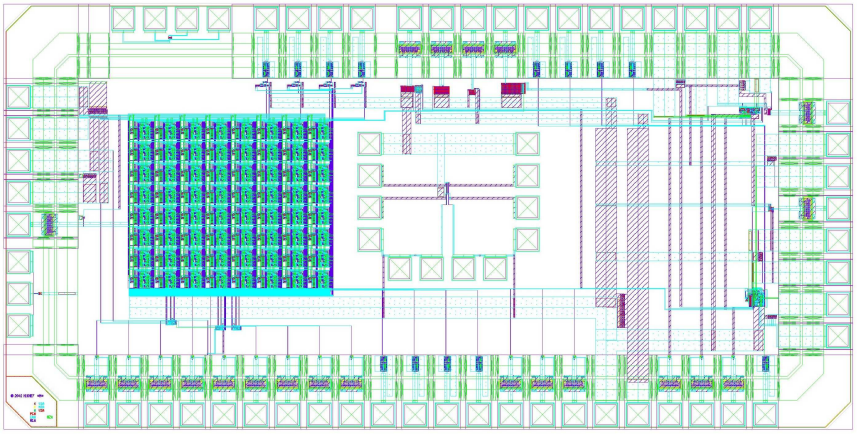

Figure 1.5: Layout of the pixADC3 prototype chip.

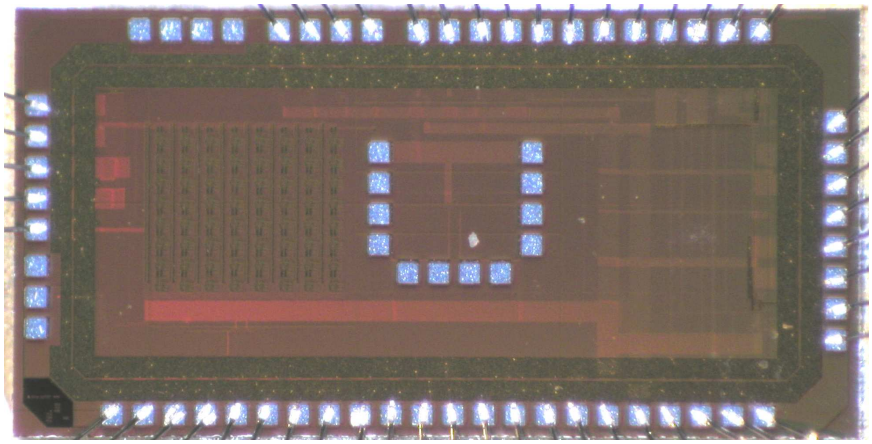

Figure 1.6: Photograph of the pixADC3 prototype chip.

The final prototype chip (pixADC4) was sent for fabrication in June 2003 also as part of a multi-project wafer. Figure 1.7 shows the layout of the chip, and figure 1.8 shows a photograph of the chip. This chip has a size of 4 mm by 4 mm and and includes an array of 16 by 16 pixels including all the circuitry discussed in this thesis. Each pixel occupies approximately 100 μm by 110 μm.

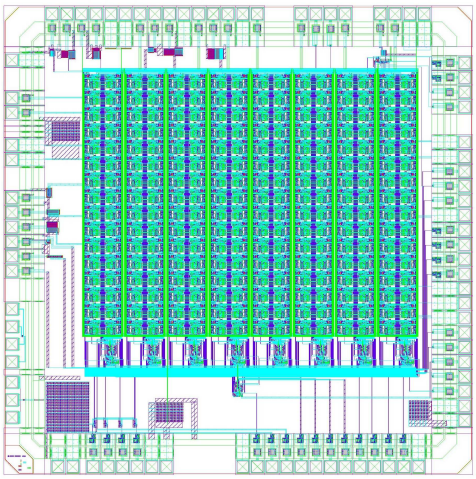

Figure 1.7: Layout of the pixADC4 prototype chip

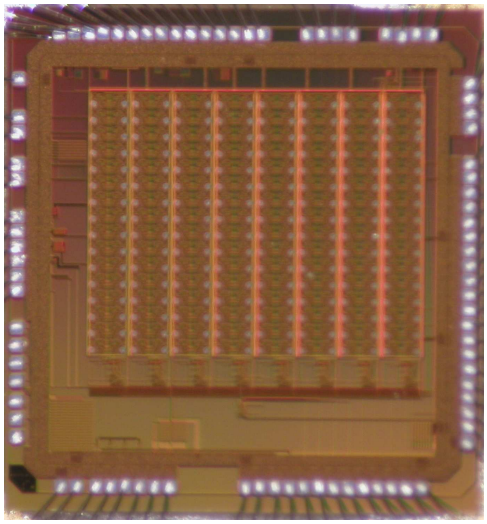

Figure 1.8: Photograph of the pixADC4 prototype chip.

1.3 Outline of the chapters

Chapter 2 gives an overview of the nature of X-rays and gamma-rays, how they are generated, how they interact with matter and which techniques can be used to detect them.

Chapter 3 offers an introduction to semiconductor-based radiation detectors. This chapter explains the processes of charge generation and charge collection in detectors based on semiconducting materials and presents the most important position sensitive semiconductor-based detectors. Hybrid pixel detectors for photon counting are also presented in this chapter to acknowledge that this thesis is an extension of other work done with these devices in the last years.

Chapter 4 gives an overview of the full system described in this thesis. The chapter starts by arguing that using analog-to-digital converters (ADCs) at the pixel level is the best way to build a pixel detector readout chip to be used for spectroscopic imaging. Then, the different components of the system are introduced in order to get a global idea of how the system works. The following chapters will explain each block in more detail.

Chapter 5 explains the design of the front-end circuits that process the signal from the detector before the analog-to-digital conversion. The input amplifier that integrates the current from the detector is described first. The second block is the hit detector, that indicates to the other blocks that a photon has hit the pixel. The last block explained in this chapter is the circuit that holds the result of the current integration in order to be processed by the ADC.

Chapter 6 describes the design of the ADCs located in the pixels. Two types of ADCs have been investigated: a successive approximation ADC and an algorithmic ADC. The design of each ADC is described, along with measurements on prototype chips.

Chapter 7 explains the architecture used to read the data from the pixels (the output of the ADC and the pixel address) as well as to select the pixels to be read out. The pixel selection is based on a double-column token ring architecture, and the data is read from the pixels using current-mode signaling.

Chapter 8, finally, offers some general conclusions and remarks, as well as pointing out some directions for further research in this area.

Bibliography

[1] A. Assmus. Early history of X rays. *Beam Line*, 25(2):10–24, 1995.

[2] J. Giersch et al. The influence of energy weighting on X-ray imaging quality. *Nuclear Instruments and Methods in Physics Research Section A*, 531(1-2):68–74, 2004.

[3] X. Llopart et al. Medipix2, a 64k pixel read out chip with 55 μm square elements working in single photon counting mode. *IEEE Transactions on Nuclear Science*, 49(5):2279–2283, October 2002.

[4] D. San Segundo Bello. Design of the bias DACs for the ALICE/LHCb and Medipix2 pixel readout chips. Internal report.

Chapter 2

X-ray and gamma-ray imaging

This chapter will introduce X-ray and gamma-ray imaging. It begins in section 2.1 with an introduction to the electromagnetic spectrum and the place that X-rays and gamma-rays have in it. The nature of X-rays and gamma-rays is explained in section 2.2, followed in section 2.3 by a brief description of the different mechanisms that can produce X-ray and gamma-ray photons. Section 2.4 will give an overview of the most important interaction mechanisms of these photons with matter.

Having introduced the basic physical mechanisms behind the generation and detection of X-ray and gamma-ray photons, the chapter will continue with an overview of the most important types of imaging systems. Section 2.5 will explain the differences between direct and indirect detection systems and section 2.6 will present the differences between integrating and quantum imaging devices. Sections 2.7, 2.8 and 2.9 will introduce detectors based on, respectively, photographic film, gas and scintillating materials. Detectors based on semiconducting materials will be explained in chapter 3.

Finally, some of the fields of application for X-ray and gamma-ray imaging will be mentioned. Section 2.10 will introduce the most important applications in medicine and biology, section 2.11 will present industrial applications of X-ray imaging and section 2.12 will briefly introduce X-ray and gamma-ray imaging in astronomy.

2.1 The electromagnetic spectrum

X-rays and gamma-rays are only two of several manifestations of electromagnetic radiation. Electromagnetic radiation transports energy through space in the form of wave packets, or energy quanta, with the energy stored in the electromagnetic field.

All forms of electromagnetic radiation can be described in terms of their wavelength (λ), frequency (ν), or equivalent energy (E). These three quantities are related by the following expression:

$$E = h \cdot \nu = h \cdot \frac{c}{\lambda} \tag{2.1}$$

where c is the velocity of the electromagnetic radiation and h is Planck's constant*.

Figure 2.1 shows graphically part of the electromagnetic spectrum. X-rays and gamma-rays are usually expressed in energy terms and the typical unit used is the *electron volt*(eV)†. The X-ray spectrum typically covers from 1 to 100 keV, while that of gamma-rays goes from about 10 to about 10000 keV. These are not the absolute limits in energy, as cosmic gamma-rays can have much higher energies (in the tens of GeV range), and some gamma-rays originating from nuclear isotopes have lower energies (for example, 5.89 keV for ^{55}Fe).

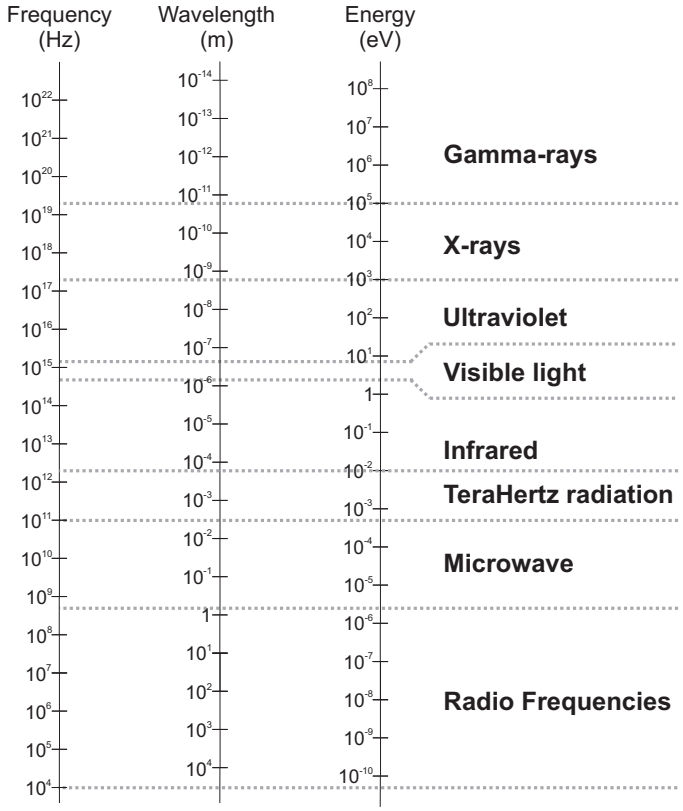

Figure 2.1: The electromagnetic spectrum. The separation between the different regimes in the figure is arbitrary and only drawn to give an idea of the order of magnitude covered by each type of radiation.

2.2 The nature of X-rays and gamma-rays

X-rays and gamma-rays appear as a result of different processes which involve the loss of surplus energy in an atom after a nuclear transition (gamma-rays)

*h = $6.626068 \cdot 10^{-34}$ m^2 kg/s
†1 eV = $1.602177 \cdot 10^{-19}$ J

or an interaction in the extranuclear electron shells (X-rays). Photons can also be emitted when a charged particle is accelerated.

2.2.1 X-rays

Electrons orbiting around the nucleus in an atom occupy well-defined energy levels or states. These levels, sometimes referred to as *shells*, are designated by the letters K, L, M, N, etc. as they become further and further removed from the nucleus. Vacancies in the electron shells can appear as a result of electron capture, internal conversion, ion/electron bombardment or photoelectric effect. These vacancies are filled either in a radiative process (ejection of a fluorescence X-ray photon) or in a non-radiative process (ejection of an electron as a result of an Auger or a Coster-Krönig transition*). For high atomic number elements, emission of fluorescence X-ray photons is more probable than emission of Auger electrons.

Electromagnetic radiation in the X-ray energy range can also be the result of *bremsstrahlung radiation*†. Bremsstrahlung radiation is electromagnetic radiation produced when a charged particle, such as an electron, accelerates or decelerates when deflected by another charged particle, such as an atomic nucleus. *Synchrotron radiation* is a special case of bremsstrahlung radiation emitted when the charged particle is accelerated in a magnetic field (see section 2.3.1).

2.2.2 Gamma-rays

The loss of energy in the nucleus of an atom due to a nuclear transition can result in alpha decay (emission of an alpha particle composed of two neutrons and two protons), beta decay (emission of an electron or a positron), spontaneous fission or gamma decay [1]. Of all these processes, only gamma decay doesn't lead to a change in the number or type of nucleons in the nucleus. The only effect of gamma decay is the loss of the surplus excitation energy via emission of gamma-ray photons, pair production or internal conversion. In *pair production* the excess energy is converted into an electron and a positron, which are emitted together. In *internal conversion* the energy is transferred to an extranuclear electron from the same atom, which is ejected from the atom.

Another source of electromagnetic radiation in the gamma-ray energy range is *annihilation radiation*, where two photons are produced as a result of the annihilation of one particle with its anti-particle. In the case of electron-positron annihilation, both photons radiate from the point of annihilation in almost exactly opposite directions, each carrying an energy equal to the rest energy of the electron‡.

*These two transitions concern three orbitals. When the principal quantum numbers of the first and the second orbitals are different, it is called an Auger transition; when they are the same, it is called a Coster-Krönig transition. For example, in a typical Auger transition an electron from the L shell drops into a vacancy created in the K shell. The energy released liberates one of the remaining electrons in the L shell. In a Coster-Krönig transition the vacancy is filled by an electron from a higher sub-shell of the same shell. We will refer to the ejected electron in both cases as *Auger electron*.

†Bremsstrahlung is German for "braking radiation".

‡The rest energy of the electron is: $E_{re} = m_e c^2$ =511 keV

2.3 Sources of X-ray and gamma-ray photons

Photons in the X-ray energy range can be produced in synchrotron rings or X-ray tubes. Gamma-rays are typically emitted by nuclear isotopes. Both X-rays and gamma-rays can also be emitted by astronomical sources, and it has recently been reported that they are also emitted in lightning phenomena [2].

2.3.1 Synchrotron radiation sources

A *synchrotron* is a particle accelerator which, by using bending magnets, causes a charged particle (typically an electron) to travel round the machine at a progressively increasing momentum in a polyhedral path. The bending of the particle beam at the vertices of the polyhedron produces a transverse acceleration and consequently a loss of energy of the particle in the form of bremsstrahlung radiation [3]. The acceleration of the particle is produced in a special device, called *cavity*, which is arranged on the particle path and provides an alternating electromagnetic field.

The name *synchrotron* refers to the fact that the strength of the magnetic field of the bending magnets is *synchronously* increased during the process of acceleration, in order to keep the particles in orbit.

The most important characteristics of synchrotron sources are wavelength tunability, very high brightness and pulsed beam. This last feature is specially interesting as it allows time resolved studies down to the femtosecond region. In order to overcome the limitations of currently operating sources in pulse duration and photon flux, new synchrotron sources are under investigation, such as using linear accelerators instead of storage rings as the source of electrons [4], and free electron lasers [5].

2.3.2 X-ray tubes

In an *X-ray tube* electrons emerge from a heated filament (cathode) and are accelerated by an electric field onto a target (anode) which is fixed at a steep angle with respect to the incoming electron beam. Approximately 98 percent of the energy from the electrons impacting on the target goes into producing heat and the rest results in both bremsstrahlung and fluorescence (also called characteristic) X-ray photons. The atomic number of the anode target material determines the amount of bremsstrahlung produced and the energy of the characteristic radiation. The element most commonly used as target is Tungsten (W), but other elements such as Molybdenum (Mo), Copper (Cu), Chromium (Cr), etc. are also used. The photon intensity can be increased by focusing the electrons onto a smaller target area or by increasing the power on the target. To avoid melting the target, it can be cooled or rotated.

2.3.3 Nuclear isotopes

In most practical gamma-ray sources, excited nuclear states are created in the decay of a parent radionuclide. Beta decay leads to the population of these excited states in the daughter nucleus. This beta decay is a relatively slow process characterized by a half-life of hundreds of days or longer, whereas the excited states in the daughter nucleus have a much shorter average lifetime

(picoseconds or less). De-excitation of the daughter nucleus takes place by emitting a gamma-ray photon whose energy is essentially equal to the difference in energy between the initial and final nuclear states. The resulting gamma-rays therefore appear with a half-life characteristic of the parent beta decay, but with discrete energies that reflect the energy-level structure of the daughter nucleus.

Gamma-ray sources based on beta decay are generally limited to energies below a few MeV. If gamma-rays with higher energies are needed, other processes based on nuclear reactions must lead to the population of higher-lying nuclear states [6].

2.3.4 X-ray and gamma-ray astronomical sources

X-rays in astronomical objects are typically produced by bremsstrahlung and Compton scattering. Cosmic gamma-ray photons can appear in particle-particle collisions, matter-antimatter annihilation, radioactive decay or in the acceleration of charged particles.

The most common situation for bremsstrahlung emission is called *thermal bremsstrahlung* and results when electrons collide with the nuclei of atoms inside a hot gas due to their random thermal motions. *Non-thermal bremsstrahlung* can also happen, and it occurs when a beam of particles decelerates on encountering an obstacle. For non-relativistic electrons* the radiation associated with the acceleration experienced as they spiral in a magnetic field is called *cyclotron radiation*. In most common astrophysical objects, free electrons move at a speed close to the speed of light, and in this case the energy spectrum of the resulting *synchrotron radiation* is spread in a way that depends on the momentum of the particle in the direction perpendicular to the field. Both synchrotron and cyclotron emission apply only to particle motion perpendicular to the direction of a magnetic field. Gases also have particle motions parallel to the field, and radiate ordinary thermal bremsstrahlung from this component of their motion.

Low energy photons (UV, optical, or below) can also scatter with relativistic electrons, producing X-ray and/or gamma-ray photons. This mechanism should be called "inverse Compton scattering" to differentiate it from classical Compton scattering (explained in section 2.4.2), but this distinction is often not made by astronomers.

As a result of a collision between a high-energy proton or cosmic ray and another proton or atomic nucleus, one or more neutral pi mesons (also called pions) may be produced. Neutral pions are unstable particles that decay into a pair of gamma-ray photons. Since the pion is usually moving at a high velocity as a result of its violent birth, the resulting gamma-rays have a broad spectrum of energies (all greater than half the pion rest mass (72 MeV), which reflects the energies of the incident particles.

In a *matter-antimatter annihilation process* a particle and its anti-particle collide and produce neutral pions which quickly decay into gamma-ray photons.

Observation of gamma-rays appearing as a result of radioactive decay confirms that the excited states of nuclei are being produced, while the measured fluxes and spectra identify the specific nuclei and the rate of their excitation. Extreme physical conditions are required to produce excited nuclei, and thus

*Particles, such as electrons in this case, are referred to as *relativistic* when their speed is close to the speed of light.

radioactive gamma-ray sources in space are associated with violents events of nucleosynthesis, such as supernovae.

2.4 Interaction of photons with matter

In general, photons interacting with matter can be completely absorbed, scattered or they might pass through the material without changes in their energy or direction. The probability that a photon will suffer an interaction is approximately proportional to E^{-3}, with E being the energy of the photon.

The most important interaction processes are the *photoelectric effect*, *incoherent scattering* and *coherent scattering*. Photons can also be converted into heat, due to the stimulation by the photons of the modes of vibration (phonons) in the lattice of the target material. For high energy photons ($E > 1$ MeV), *pair production* and other nuclear reactions such as photo-nuclear absorption also play a role in the absorption or scattering of photons [7]. The combined effect of all these processes in a photon beam is described by the *mass attenuation coefficient*.

2.4.1 The photoelectric effect

The photoelectric effect describes how a photon of energy E_p interacts with an absorber atom and disappears completely, transferring its energy and momentum to an electron from one of the shells of the absorber atom. The ejected photo-electron has an energy of:

$$E_e = E_p - E_B \tag{2.2}$$

where E_B represents the binding energy of the electron in its original shell.

The atom, ionized by having lost one of its innermost electrons, is left in a highly excited state. If the vacancy has occurred in any orbital beneath the valence shell, then a rearrangement of the electrons in all the orbitals above the vacancy will occur, with electrons from higher orbitals cascading down to fill in the hole. This rearrangement can result in emission of fluorescence X-ray photons or Auger electrons.

2.4.2 Incoherent scattering

Incoherent scattering (also referred to as *Compton scattering*) is an inelastic scattering of a photon with one electron of the absorbing material. In contrast to the photoelectric effect, in a Compton interaction the photon loses only part of its energy and momentum to the photo-electron. The energy E_{ps} of the scattered photon depends on the scattering angle and it is given by:

$$E_{ps} = \frac{E_{pi}}{1 + \frac{E_{pi}}{m_e \cdot c^2}(1 - \cos\theta)} \tag{2.3}$$

and that of the ejected photo-electron by:

$$E_e = E_{pi} - E_{ps} = E_{pi}\left(\frac{\left(\frac{E_{pi}}{m_e \cdot c^2}\right)(1 - \cos\theta)}{1 + \left(\frac{E_{pi}}{m_e \cdot c^2}\right)(1 - \cos\theta)}\right) \tag{2.4}$$

where E_{pi} is the energy of the incident photon, m_e is the rest mass of the electron, c the speed of light, and θ is the angle between incident and scattered photons.

The angle at which the photon is scattered can take on any value and the energy imparted to the photo-electron has a continuous distribution from zero to a maximum energy (E_{max}) which defines the *Compton edge*, and corresponds to the case of the photon being backscattered at an angle θ of 180 degrees:

$$E_{\max} = \frac{2 \cdot E_{pi}^2}{m_e \cdot c^2 + 2 \cdot E_{pi}} \tag{2.5}$$

2.4.3 Coherent scattering

In coherent scattering there is no change in the energy of the scattered photon and only the direction of the photon is changed. This type of scattering is also called *Rayleigh scattering*. The physical mechanism is coherent scattering on many atoms of a regular crystal lattice, so the recoil momentum is taken by the whole lattice and therefore negligible.

Diffraction in a crystal is the result of a series of events that involve both coherent scattering and interference.

2.4.4 Pair production

Pair production refers to the creation of an elementary particle and its antiparticle, usually from a photon (or another neutral boson). In nuclear physics, this occurs when a high-energy photon interacts in the vicinity of a nucleus, allowing the production of an electron and a positron pair without violating conservation of momentum. To create an electron-positron pair, the energy of the interacting photon has to be at least twice the rest energy of the electron*. In most cases, the positron will later annihilate with an electron, emitting a pair of photons in opposite directions, each with an energy of approximately 511 keV.

2.4.5 The mass attenuation coefficient

If a photon beam with an intensity of $I_0(E)$ photons per second strikes a slab of material with thickness dx the absorbed beam intensity ($dI(E)$) can be calculated using the Beer-Lambert law:

$$\frac{dI\,(E)}{I_0\,(E)} = -\mu\,(E) \cdot dx \tag{2.6}$$

where $\mu\,(E)$ is the *linear attenuation coefficient*, which represents the fraction of incident photons interacting with the material per unit length. The linear attenuation coefficient accounts for the various interactions that occur in the material and it is composed of four major components:

$$\mu\,(E) = \mu_{ph}\,(E) + \mu_{coh}\,(E) + \mu_{inc}\,(E) + \mu_{pp}\,(E) \tag{2.7}$$

where $\mu_{ph}\,(E)$ is the photoelectric absorption coefficient and describes the photoelectric effect, $\mu_{coh}\,(E)$ is the total coherent scattering coefficient, $\mu_{inc}\,(E)$ is

*The rest energy of the electron is approximately equal to 511 keV.

the total incoherent scattering coefficient and $\mu_{pp}(E)$ describes the effect of pair production.

The photoelectric absorption coefficient ($\mu_{ph}(E)$) includes the probability of ionizing all the electron shells in an atom, and it can be broken down into a sum of the probabilities of ionizing each shell. If the energy of the photon is less than that required to ionize a particular shell [8], then the term for that shell will be zero, causing an abrupt discontinuity in $\mu_{ph}(E)$ at this energy. These values are characteristic for each element. For example, figure 2.2 shows the mass attenuation coefficient as a function of the photon energy for silicon. The discontinuity corresponding to the K-shell, referred to as *K-edge* is clearly visible at 1.8389 keV.

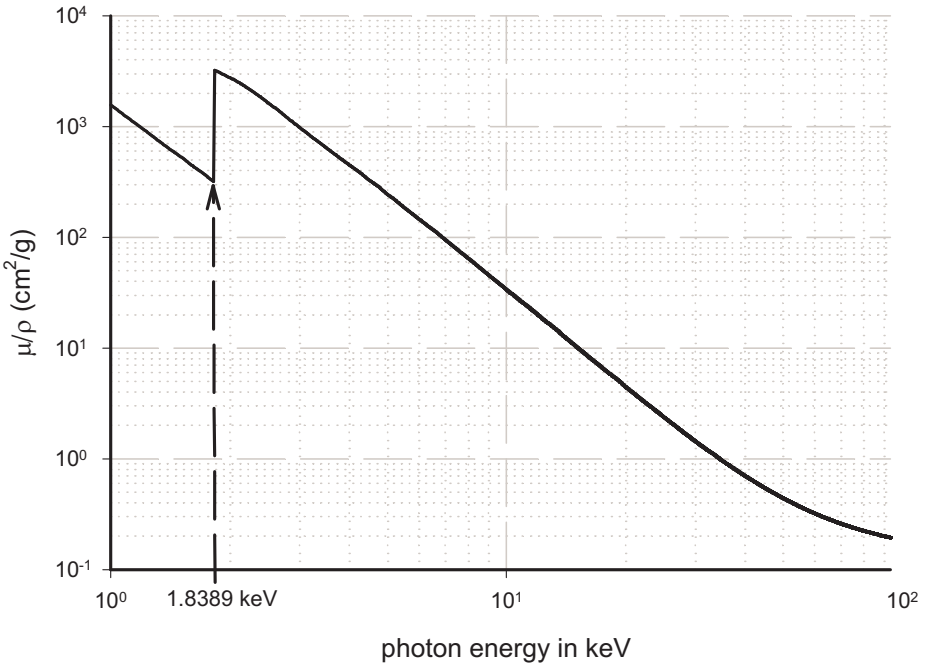

Figure 2.2: Mass attenuation coefficient as a function of the photon energy for silicon showing the K-edge discontinuity at 1.8389 keV.

The transmitted intensity of photons that have not suffered interactions with the material is given by integrating Equation 2.6 over a finite thickness x:

$$I(E,x) = I_0(E) \cdot e^{-\mu(E)\cdot x} \tag{2.8}$$

The linear attenuation coefficient μ depends on the density of the material suffering the photon interaction. As a consequence, the mass attenuation coefficient (μ/ρ, with ρ the density of the absorber material) is more frequently used.

Figure 2.3 [9] shows the relative attenuation of photons in silicon due to the different interaction mechanisms explained earlier.

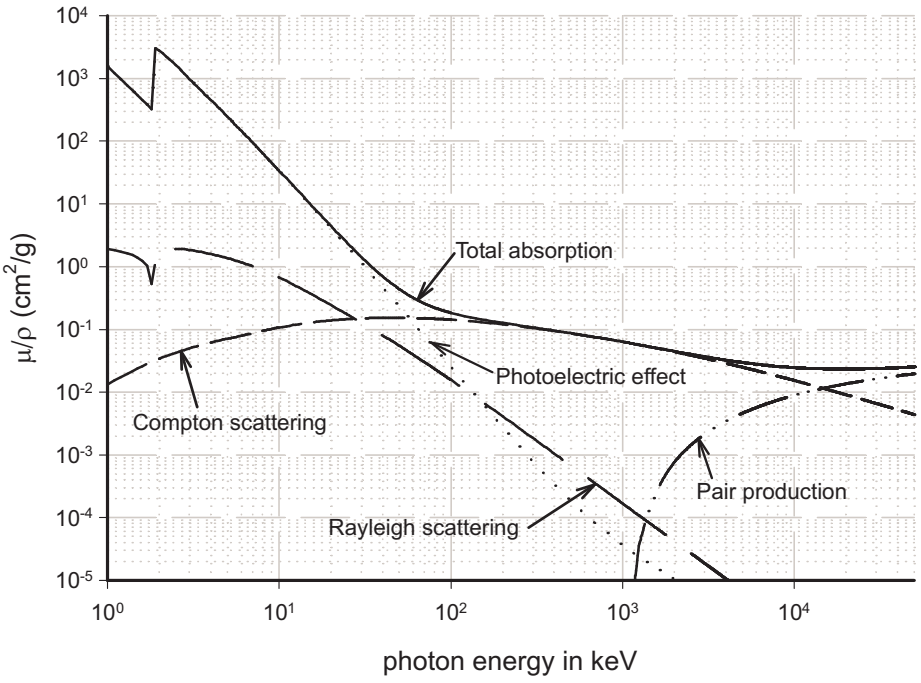

Figure 2.3: Mass attenuation coefficients for the photoelectric effect, Compton scattering, Rayleigh scattering and pair production for silicon, as a function of the photon energy.

2.5 Direct and indirect detection

When a charged particle such as an electron or a charged ion interacts with a detector, it loses its energy by many sequential interactions; and it is mainly through ionization of the orbital electrons within the target atoms that it slows down gradually.

Photons are uncharged particles and hence cannot ionize directly the detector. They must first interact with the material and transfer all or part of their energy to a photo-electron, which will lose its energy by sequential interactions.

In *direct detection* systems the resulting photo-electron is slowed down by ionization and generates pairs of positive and negative electrical charge in the detector volume. This charge can be measured to determine the energy of the interacting photon.

The result of the ionization process by the photo-electron in *indirect detection* systems is the generation of visible light photons which are subsequently detected with a (separate) conventional visible light sensor.

2.6 Integrating and quantum imaging systems

The final quantity measured in any type of imaging detector is the charge generated by the primary photo-electron in direct detection systems or by the secondary visible light photons in indirect detection systems.

In *integrating systems*, the total charge released in each interaction is accumulated during the exposure time in the sensor. At the end of the exposure time the accumulated charge is measured, giving an estimation of the total energy absorbed by the detector. However, the noise charge generated in the sensor is also accumulated during the exposure time, and as a result the signal-to-noise ratio and the dynamic range are reduced.

The charge generated in the sensor of a *quantum imaging system* is measured and processed for each interaction. The simplest quantum imaging devices are *photon counting* systems, where the signal from each interaction is compared to a certain threshold, and if the signal exceeds this threshold the value of a counter is incremented. The possibility to set a threshold implies that noise as well as background (Compton scattered events, X-ray fluorescence background in synchrotron experiments, etc.) can be eliminated.

Because of the signal processing needed in quantum imaging systems (signal conditioning and threshold comparison), there is a *dead time* during which no further photon interactions can be processed. Due to this inherent dead-time in quantum imaging systems, integrating systems have a better efficiency than quantum imaging systems for high photon rates (in the order of 10^{12} photons per mm^2 and second or higher).

2.7 Film-based detectors

Film-based detectors use emulsions composed of gelatin containing grains of a silver halide compound deposited on either glass or a flexible support. When the energy from the impinging photons is absorbed by the silver halide grains, electrons are released from the atoms. These electrons slow down and are eventually captured at trapping centers within the grains. These centers attract

more and more electrons during exposure and contain the latent image. Film development amplifies the chemical reduction of the illuminated grains into black metallic silver.

The main advantage of film-based systems is their excellent spatial resolution, which is mainly limited by the thickness of the sensitive emulsion (approximately between 20 μm and 1 mm) and the grain size (about 1 μm in diameter). The biggest disadvantages of these detector systems are their limited dynamic range, long read-out time and non-linear response. Additionally, a sheet of emulsion has a poor absorption efficiency for X-rays. Due to these limitations, and in spite of their high spatial resolution, this is the main reason why direct exposure films are practically not in use except for very special cases (e.g. the CHORUS experiment [10]). Film detectors are, however, used widely in conjunction with scintillation detectors.

2.8 Gas-filled detectors

A basic gas-filled detector consists basically of a sealed chamber containing a gas and two electrodes of opposite polarity[11, 12]. When a photon enters the gas volume, a photo-electron is created following an interaction with one of the molecules of the gas. This photo-electron will subsequently create pairs of electrons and positive ions by ionization. If an electric field is applied between the two electrodes, the electrons will be collected in the anode and the positive ions in the cathode.

There are three basic modes of operation for gas-filled detectors depending on the strength of the electric field: ionization chambers, proportional counters and Geiger counters. In an *ionization chamber*, the number of positive ion-electron pairs created by the photo-electron is directly proportional to the kinetic energy transferred by the photon and inversely proportional to the ionization energy of the gas. If the electric field in an ionization chamber is high enough, the detector works as a *proportional counter* and the electrons migrating to the anode can acquire sufficient kinetic energy between collisions to cause further ionization of the gas molecules. The electrons produced in this secondary ionization are in turn accelerated towards the anode and can produce further ionization, so that an avalanche of electrons and positive ions results. The total resulting ionization charge is nevertheless still proportional to the initial photon energy. If the electric field is further increased, the amount of charge collected becomes independent of the amount of initial ionization: each primary event causes an avalanche of secondary ions extending throughout the whole volume and the detector works as a *Geiger counter*, where the measured quantity is the number of events and not the absorbed energy.

2.9 Scintillation detectors

The operational principle of this type of detectors is the detection of the scintillating light produced in certain materials by ionization and subsequent recombination of charge carriers [11]. This light can be detected directly by storage phosphors [13], flat-panel detectors [14, 15], CCD sensors [16], CMOS imaging detectors [17] or amplified by photomultiplier tubes [11]. The generated scintil-

lating light can also be guided for some distance by internal reflection in fibers until the image sensor in order to shield the sensor from the radiation.

Scintillation detectors are widely used because the scintillator material can be made large and of any geometry. The density of the material also allows to obtain good detection efficiency.

2.10 Applications in medicine and biology

The applications of X-ray and gamma-ray imaging in medicine and biology are very wide and developments in these fields are continuously happening. A very broad classification of these applications distinguishes between *transmission radiography*, *biomedical and biological structural analysis* and *emission radiography*.

In *transmission radiography* the patient is illuminated with a (wide spectrum) X-ray beam and an image is taken of the transmission of parts of the body with different densities. The photon energies used in transmission imaging range from around 10-30 keV for mammography up to 70-100 keV for dental and chest radiography.

Biomedical and biological structure analysis use the diffraction patterns created by the X-ray photons illuminating the object under investigation after being coherently scattered by the electron clouds of the atoms in the sample [18, 19].

Emission radiography is based on the detection of photons emitted by a radioisotope which has been introduced in the subject under investigation. Usually one distinguishes between emission radiography in vivo (single photon emission computer tomography (SPECT) [20] or positron emission tomography (PET) [21]) and autoradiography (used for a specimen on the microscopic scale). The information desired in both cases is the spatial distribution of the source in order to study the physiology of different tissues. The radioisotope is present in a drug injected into the patient in SPECT or in a labelled molecule in autoradiography, and the detector is sensitive to the direct emission of a photon by the radioisotope. PET is based on the detection of back-to-back photons from the annihilation of positrons emitted by the drug with electrons in the neighboring tissue. In all cases the drug is chosen according to the metabolism of the tissue under study and is detected owing to its high specific activity in this tissue.

2.11 Industrial applications

In contrast to many other methods for investigating the properties of materials, X-rays provide a way to look at the samples in a non-destructive way and can be applied to obtain information about the structure and composition of materials at different scales [22, 23, 24].

Information about the chemical elements that are present in the material and their concentrations can be obtained by using X-ray fluorescence. In these cases, the wavelengths or energies of fluorescence emission lines are measured to establish the elemental composition of a sample [25, 26].

X-ray generated diffraction patterns can be used to study the microscopic structure of solid materials [27].

Transmission imaging [28] is used in general for studying the macroscopic structure of the materials: measuring the thickness and depth of solid homogeneous materials, examining the structure of metal and similar objects and for security screening. A new technique in this area is *phase contrast imaging*, which records information from the bending (or refraction) of X-rays, which occurs as they pass through the item being studied. The refraction effect occurs because denser materials change the speed of the X-rays more than lighter ones, producing what is known as a phase shift, which can greatly increase the edge-contrast between materials of comparable density [29].

2.12 Applications in astronomy

Most extra-terrestrial X-rays and gamma-rays must be detected from spaceborne telescopes because they are absorbed in the Earth's atmosphere. Only the highest energy gamma-rays (with energies above 50 GeV) can be observed from the surface of the earth by means of the particle showers they initiate in the upper atmosphere [30].

2.13 Summary

X-ray photons appear as a result of different processes in the extranuclear electron shells, such as electron capture, internal conversion, ion/electron bombardment or photoelectric effect. Gamma-ray photons appear as a result of energy loss in the atomic nucleus. Although the two types of photons have different origins, the way they interact with matter and the systems used to detect them are the same.

Photons can interact with matter in different ways, transferring all or part of their energy to the material. The most important interaction mechanisms for X-ray and gamma-ray photons are the *photoelectric effect*, *incoherent or Compton scattering*, *coherent or Rayleigh scattering* and *pair production*.

The systems used to measure X-ray and gamma-ray photons can be classified by the detection mechanism (direct or indirect), the signal processed (integrating or quantum imaging) or the detector material (film, gas, scintillator, semiconductor). These detector systems are used in many different applications in medicine, material analysis and astronomy.

Bibliography

[1] G. Gilmore and J. Hemingway. *Practical gamma-ray spectrometry.* John Wiley and sons, 1995.

[2] L. Wright. X-Rays Abound When Lightning Strikes. *Scientific American*, January 2003.

[3] H. Winick (ed.). *Synchrotron radiation sources : a primer.* World Scientific, 1994.

[4] S.M. Gruner and D.H. Bilderback. Energy recovery linacs as synchrotron light sources. *Beam Line*, 32(1):22–31, 2002.

[5] C. Pellegrini and J. Stöhr. X-ray free electron lasers. *Beam Line*, 32(1):32–41, 2002.

[6] G.F. Knoll. *Radiation detection and measurement*. Wiley, 3rd edition, 2000.

[7] E.G. Fuller and E. Hayward. *Photonuclear Reactions*. Dowden, Hutchinson & Ross, 1976.

[8] http://xray.uu.se/hypertext/EBindEnergies.html.

[9] http://www-nds.iaea.org/reports/nds-195.htm.

[10] http://choruswww.cern.ch/.

[11] W.R. Leo. *Techniques for Nuclear and Particle Physics Experiments*. Springer Verlag, 1987.

[12] A. Sharma. Gaseous micropattern detectors in astrophysics, radiology and plasma physics. In *Proceedings of the IEEE Nuclear Science Symposium and Medical Imaging Conference, Lyon, October 15-20 2000*, volume 1, pages 210–213.

[13] J.-M. Spaeth. Recent developments in X-ray storage phosphor materials. *Radiation Measurements*, 33(5):527–532, 2001.

[14] J.-P. Moy. Recent developments in X-ray imaging detectors. *Nuclear Instruments and Methods in Physics Research Section A*, 442(1-3):26–37, 2000.

[15] M.J. Yaffe and J.A. Rowlands. X-ray detectors for digital radiography. *Physics in Medicine and Biology*, 42:1–39, 1997.

[16] X. Badel et al. Improvement of an X-ray imaging detector based on a scintillating guides screen. *Nuclear Instruments and Methods in Physics Research Section A*, 487(1-2):129–135, 2002.

[17] M.A. Abdalla et al. An integrating CMOS APS for X-ray imaging with an in-pixel preamplifier. *Nuclear Instruments and Methods in Physics Research Section A*, 466(1):232–236, 2001.

[18] R.A. Scott. Biological Applications of Synchrotron Radiation. *Beamline*, 24(3/4):19–28, 1994.

[19] J.P. Abrahams et al. Area detectors in structural biology. *Nuclear Instruments and Methods in Physics Research Section A*, 509(1-3):274–282, 2003.

[20] F.J. Beekman et al. High-resolution emission tomography of small laboratory animals: physics and gamma-astronomy meet molecular imaging. *Nuclear Instruments and Methods in Physics Research Section A*, 509(1-3):229–234, 2003.

[21] P.K. Mardsen. Detector technology challenges for nuclear medicine and PET. *Nuclear Instruments and Methods in Physics Research Section A*, 513(1-3):1–7, 2003.

[22] A. Bienenstock and A.L. Robinson. Impact of synchrotron radiation on materials research. *Beam Line*, 25(2):35–44, 1995.

[23] G.S. Cargill III. Novel applications of X-ray analysis to microelectronic materials and devices. *Solid-State Electronics*, 46(8):1139–1143, 2002.

[24] V. Kogan et al. Applying X-rays in material analysis. *Nuclear Instruments and Methods in Physics Research Section A*, 509(1-3):290–293, 2003.

[25] K.H.A. Janssens and F.C.V. Adams. *Microscopic X-ray fluorescence analysis*. Wiley, 2000.

[26] R. Jenkins. *X-ray fluorescence spectrometry*. Wiley, 1999.

[27] M.M. Woolfson. *An introduction to X-ray crystallography*. Cambridge University Press, 1997.

[28] E. Lifshin. *X-ray characterization of materials*. Wiley, 1999.

[29] Jan Jakubek. Data processing and image reconstruction methods for pixel detectors, 2006. Presented at the 2006 IWORID workshop in Pisa.

[30] R. A. Remillard. X-ray detectors for astrophysics. *Nuclear Instruments and Methods in Physics Research Section A*, 531:285–291, 2004.

Chapter 3

Semiconductor-based detectors for radiation imaging

The previous chapter has shown that X-ray and gamma-ray photons can be detected with film, gas or scintillator-based detectors. This chapter will take a deeper look into semiconductor-based radiation detectors, as they are proving to be very efficient and their use is growing in many different fields*.

This chapter begins with a brief review of the processes of charge generation and collection in sections 3.1 and 3.2. Section 3.3 will look at the concept of energy resolution. Section 3.4 introduces reversed-biased pn junction detectors, as they are the most commonly used type of semiconductor-based radiation detector. Section 3.5 gives a short overview of what are the characteristics needed in a semiconducting material to be used as a radiation detector. Section 3.6 presents the different types of position sensitive detectors and section 3.7 introduces photon-counting hybrid pixel detectors.

3.1 Charge generation

The minimum energy needed by a photon to free an electron in a semiconductor is equal to the band-gap energy separating the conduction band from the valence band. For example, a visible light photon can break one of the covalent bonds in a semiconductor via a photoelectric interaction, exciting an electron into the conduction band and leaving a hole in the valence band [1]. The actual energy needed to create electron-hole pairs is the *ionization energy* or mean energy per ionization, and its value is typically above the band-gap energy of the material, as other mechanisms are involved in the electron-hole pair creation [2].

Photons with high energy can also free an electron located in one of the shells closer to the nucleus. The kinetic energy acquired by this *photo-electron* will be spent in the generation of secondary electron-hole pairs by ionization, and the vacancy left by the photo-electron will be filled by an electron falling from a

*The reader is supposed to be acquainted with the basic physics of semiconductor devices. A good reference is [1].

higher shell. The secondary electrons and holes generated by the photo-electron can create further ionization if their energy is high enough or else occupy the conduction band (electrons) and the valence band (holes).

3.2 Charge collection

Under normal circumstances, after the photon interaction and the generation of the electron-hole pairs, the electrons in the conduction band would eventually de-excite and recombine with the holes present in the valence band to restore charge equilibrium.

To avoid recombination and to collect the charge generated by the photon interaction, two electrodes with a negligible potential barrier (ohmic contact) can be added to the semiconducting material. If an electric field is applied between the electrodes, the carriers will be forced to migrate up (electrons) or down (holes) the field gradient and be collected at the electrodes. Before reaching the electrodes, the electrons and holes may recombine or be trapped at trapping centers such as lattice defects or impurities of the crystal. The concentration of these recombination traps determines the lifetime of the carriers.

In most semiconductor materials used in radiation detection the constant flow of carriers due to the applied electric field will degrade the performance of the detector. In order to reduce this DC current, a potential barrier can be added at one (or both) of the contacts, so that the carriers cannot flow freely between the two electrodes. Reverse-biased *Schottky contacts* (metal-semiconductor junctions) and *pn junctions* are used for this purpose. In both cases the charge carriers initially removed by the applied electric field are not replaced at the opposite electrode, and consequently their overall concentration within the semiconductor drops. The current flowing between the electrodes is thus reduced to a sufficiently low value which allows the detection of the current created only by the electron-hole pairs resulting from the photon interaction. Semiconductor materials with high resistivity (such as CdZnTe, diamond and others) can nevertheless be used in ohmic mode (i.e. using only ohmic contacts), as their DC current is low enough.

3.3 Energy resolution

The charge generated by the photo-electron and collected at the electrodes will be used as a measure of the energy deposited by the photon in the detector. The average energy lost by the photo-electron to produce one electron-hole pair is the most important characteristic of a semiconductor-based detector, and it is called *ionization energy* (ϵ). The ionization energy is related to the *quantum yield* (N), or number of electron-hole pairs created, by the following expression:

$$N = \frac{E_0}{\epsilon} \tag{3.1}$$

where E_0 is the kinetic energy carried by the photo-electron.

If all the incident (and not reflected) energy can be accounted for in terms of the generated electron-hole pairs and lattice vibrations, the value of the ionization energy can be considered as the sum of three contributions: the intrinsic band-gap, the optical phonon losses and the residual kinetic energy [3, 4].

The *phonon losses* appear because the charge carriers capable of producing electron-hole pairs are coupled to optical lattice modes and can also emit Raman phonons. The *residual kinetic energy* arises from the fact that the deposition of energy culminates in the production of electrons and holes unable to induce further ionization and, consequently, bound to convert their residual (kinetic) energy into lattice vibrations.

The measured spectrum of a mono-energetic source results in a peak centered at the source energy. The energy resolution of a radiation detector (ΔE) is typically given in terms of the full width at half maximum (FWHM) of this peak in the spectrum.

In the absence of nuclear interactions, the energy resolution of a pulse-height spectrum line in a semiconductor-based detector reflects an addition in quadrature of the statistical spread in the generation of electron-hole pairs (Δ_{gen}), the loss fluctuations occurring during charge collection (Δ_{coll}) and the signal scatter injected by the amplifying system and/or the leakage current (Δ_{syst}):

$$\Delta E = \sqrt{{\Delta_{gen}}^2 + {\Delta_{coll}}^2 + {\Delta_{syst}}^2} \tag{3.2}$$

When only a fraction of the energy is deposited inside the sensitive volume of the detector, the variance in the number of generated pairs N can be determined by Poisson statistics:

$$\sigma^2(N) = \overline{N} = \frac{E_o}{\epsilon} \tag{3.3}$$

Assuming a Gaussian distribution we can calculate the intrinsic energy resolution of the detector Δ_{gen} as:

$$\Delta_{gen} = \epsilon \cdot 2 \cdot \sqrt{2 \cdot \ln(2) \cdot \sigma^2(N)} = 2.355 \cdot \sqrt{E_o \cdot \epsilon} \tag{3.4}$$

The actual energy resolution of radiation detectors is smaller than the value given by Equation 3.4. The upper limit to the obtainable energy resolution is imposed by the fluctuations in the number of positive and negative charge carriers created by the ionizing radiation. Fano was the first to discuss this for ionization in gases [5] and he found that the variance of the number of ion pairs generated by radiation of fixed energy is F times the mean number of charge carrier pairs. The numerical factor F is called the *Fano factor* and it is determined by the properties of the absorbing medium and by the ionization mechanism. The total number of ionizations that can occur and the energy lost in each ionization are thus constrained by this value, which is usually less than one. The reason is that the ionization events are not independent and hence Poisson statistics is not applicable. Typical values of the Fano factor for semiconducting materials are between 0.1 and 0.2.

Taking the Fano factor into account, the correct relation between the quantum yield N and its variance is:

$$\sigma^2(N) = F \cdot \overline{N} \tag{3.5}$$

And the intrinsic energy resolution can then be expressed as:

$$\Delta_{gen} = 2.355 \cdot \epsilon \cdot \sqrt{F \cdot \overline{N}} = 2.355 \cdot \sqrt{F \cdot E_o \cdot \epsilon} \tag{3.6}$$

3.4 Reverse-biased pn junction detectors

Reverse-biased pn junction detectors are the most commonly-used type of radiation detectors based on semiconductor materials. A reverse-biased pn junction can be modeled (under small signal conditions) as a capacitor in parallel with two current sources as shown in figure 3.1.

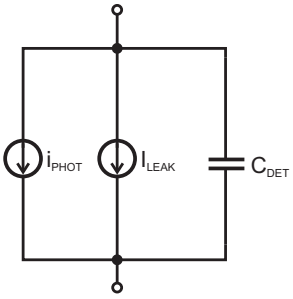

Figure 3.1: Small signal equivalent model of a reverse-biased pn-junction radiation detector

The DC current source I_{LEAK} models the leakage current, and i_{PHOT} models the transient signal resulting from the charge generated by the interaction. The leakage current consists of two main components: bulk leakage currents and surface leakage currents. *Bulk leakage* currents arise internally within the volume of the detector and are caused by the sum of two mechanisms: minority carrier current and thermal generation of electron-hole pairs within the depleted region. The latter is the more important of the two processes. *Surface leakage* effects take place at the edges of the junction, where relatively large voltage gradients must be supported over small distances.

The value of the detector capacitance C_{DET} depends on the detector dimensions and is equal to:

$$C_{DET} = A\frac{\epsilon_s}{W} \tag{3.7}$$

where A is the area of the junction, ϵ_s is the dielectric constant of the semiconducting material and W is the thickness of the depletion region in the junction. In the case of a p^+n junction, the value of W can be calculated from:

$$W = \sqrt{\frac{2\epsilon_s\left(V_{bi} + V_{rbias}\right)}{qN_D}} \tag{3.8}$$

where V_{bi} is the built-in potential of the junction, V_{rbias} is the (reverse) bias voltage applied*, q is the charge of an electron and N_D is the doping concentration of the substrate. To improve the charge collection efficiency and obtain a fast response, the depletion region is typically made to encompass the whole thickness of the detector.

*When the diode is forward biased, the sign of V_{rbias} is negative.

3.5 Semiconducting materials for radiation detection

In general, the preferred properties required for a semiconducting material to be used in a radiation detector operating at room temperature are: a high atomic number (Z) for efficient radiation atomic interactions; band-gap energy (E_g) small enough to give a large quantum yield, but also large enough for high resistivity and low leakage current; high mobilities of holes and electrons, long carrier lifetime and freedom from delayed trapping and from space charge effects to give efficient and fast collection of the charge; high purity, homogeneous and defect-free material with an acceptable cross-sectional area and thickness; and electrodes that produce no defects, impurities or barriers to the charge collection process.

Silicon is certainly the best known and most frequently used material. It has the advantages of room temperature operation, wide availability and very good homogeneity, but its low atomic number results in mediocre attenuation properties for photons with energies above 10 keV. Therefore a lot of effort has been put into the research and development of other materials [6, 7] such as semi-insulating (SI) GaAs [8], epitaxial GaAs [9], CdTe and CZT ($Cd_{1-x}Zn_xTe$) [10], SiC [11], TlBr [12], InP [13], HgI_2 [14] or PbI_2 [15].

3.6 Position sensitive detectors

Semiconductor-based position sensitive detectors can be built using different segmentation and readout schemes. If the detector is not segmented, position sensitivity can be achieved by making a pulse sharing between two or several contacts on the detector and analyzing the arrival time or the signal heights at the different contacts. If the detector is segmented, position sensitivity can be achieved by parallel or serial readout of the signal generated in each segment. The segmentation can be done either in one dimension (strip and drift detectors) or two dimensions (pixel, pad and 3-D detectors).

3.6.1 Microstrip detectors

Microstrip detectors consist of thin high-resistivity silicon sensors segmented on one side into narrow and long ion-implanted strips [16]. These strips are reverse-biased pn junctions which provide one-dimensional information about the position of the interaction. Figure 3.2 shows a simplified transversal view of a typical microstrip detector.

Several methods can be used to achieve two-dimensional resolution, such as using several layers of tilted microstrip detectors or using double-sided microstrip detectors [17]. However, in both these cases, when more than one interaction occurs simultaneously, ambiguities (ghost hits) appear. A different method is the *edge detection* method [18, 19], where the detectors are oriented edge-on with respect to the X-ray beam and are used as a linear scanning system. Two-dimensional resolution is defined in one direction by the strip pitch and in the second direction by the scanning step (typically the wafer thickness of about 300 μm). The effective absorption length is increased from a few hundred micrometers to the length of the strip (about 1 cm). A variation on this

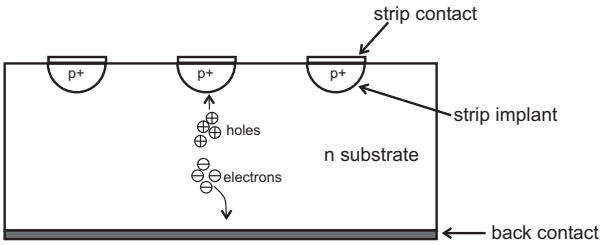

Figure 3.2: Transversal view of a single-sided microstrip detector. Not shown in the figure is the applied bias voltage.

technique is the *almost edge-on* configuration [20], where the silicon sensor is tilted by a small angle of around four degrees and illuminated either through the front- or the back-side. The tilt is done to avoid the dead layer due to the guard ring at the edge of the detector.

3.6.2 Drift detectors

In a drift detector [21, 22] pn junctions are fabricated on both sides of a high resistivity silicon wafer, and a collecting electrode (anode) is placed somewhere close to the lateral edge of the detector. A field parallel to the diode surface drains the electrons created by the photon interactions to the anodes. The anode can be segmented to achieve two-dimensional resolution. The time it takes the electron to reach the anodes from the interaction point will give the position in one direction, while the anode pitch gives the position resolution in the perpendicular direction. Figure 3.3 shows a transversal view of a drift detector.

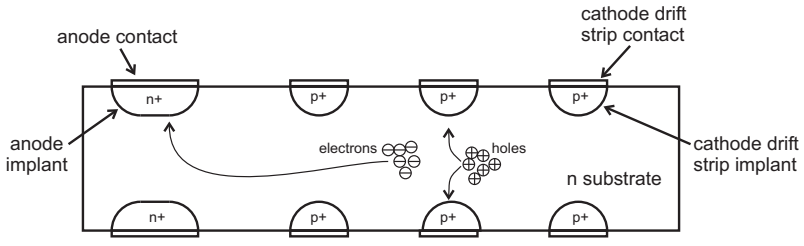

Figure 3.3: Transversal view of a drift detector.

The main limitations of drift detectors are the rather long distances that the electrons have to travel to reach the anode, which limit the particle rate, and the temperature dependance of the electron drift time. Drift detectors are also dependent on electrical field variations due to inhomogeneities in the detector substrate, which makes them not suitable for high radiation environments.

3.6.3 Pad detectors

In a pad detector a two dimensional array of diodes, each with an area of 1 mm^2 or more, is implemented in one substrate. Each diode is connected to one readout channel, typically via the detector substrate.

3.6.4 Pixel detectors

Pixel detectors are built by creating a two-dimensional array of small detector elements, with dimensions typically below 1 mm^2. In terms of integrated functionality in the pixel, pixel detectors can be divided into passive and active pixel detectors.

3.6.4.1 Passive pixel detectors

Passive pixel detectors do not include active circuitry (i.e. amplifiers, comparators, etc.) in the pixel itself, only the detecting device and in some cases also a switch.

The most important passive pixel detectors are direct conversion flat-panel systems [23]. Although direct conversion CCDs [24] and hybrid CCDs [25, 26] also exist, they are rarely used (except for infra-red space imaging). CCDs for X-ray imaging are mostly used in conjunction with scintillator detectors as explained in section 2.9. A relatively new device that is gaining popularity is the DEPFET * [27, 28].

The charge generated in the detecting device by the interaction is stored in the pixel. In CCD-based detectors the readout of the charge is done by transferring it from pixel to pixel until it reaches the periphery of the detector chip. In the other types of detectors when the pixel is selected to be read, a switch connects the pixel to the periphery of the pixel array (or in some cases another chip) for electronic processing.

3.6.4.2 Active pixel detectors

In an active pixel detector each pixel has an associated signal processing circuit inside the detection substrate or on a separate layer. In both cases, due to the low detector capacitance at the input of the processing electronics a robust, low noise system can be achieved.

Active pixel detectors can be divided into three categories depending on how the detector is integrated with the processing electronics: monolithic, SOI or hybrid pixel detectors.

Monolithic active pixel detectors have the detecting element and the processing electronics in the same substrate [29].

In *silicon-on-insulator* (SOI) based active pixel detectors [30, 31], a silicon film is grown over an insulating layer on a silicon substrate. The substrate is used as the detector and the processing electronics are integrated on the grown silicon film. The development of this type of detectors has been slowed down by the lack of affordable SOI wafers with high-quality silicon substrates.

*DEPFET stands for DEpleted P-channel Field Effect Transistor. Although this device can provide amplification due to its operation as a Field Effect Transistor, we decided to include it with the passive pixel detectors as it does not include any circuitry besides the detecting device itself.

In a *hybrid pixel detector* the sensor and the electronics cells are fabricated in different substrates. The sensor converts the photons into charge pairs with high efficiency, and an electric field collects the generated charge. The electronics chip is connected to the segmented sensor using flip-chip interconnection techniques [32]. The sizes of both the detector and the electronics elements are typically equal, but this does not always need to be the case [33]. Although hybrid pixel detectors are mostly used in quantum imaging systems (see section 3.7), integrating hybrid pixel detectors have also been developed [34].

3.6.5 3-D detectors

Unlike the previously mentioned detectors, where ion implantation and diffusion are used to create the detecting diode elements, 3-D detectors [35, 36] are created by making deep holes with a small diameter in the detector substrate. These holes can be made by dry etching, laser drilling or photochemical etching. The holes can be filled with a doped material such as polysilicon, or the walls of the holes can be doped directly and a metal is evaporated inside the holes to create the contact. Figure 3.4 shows a transversal view of a 3-D detector.

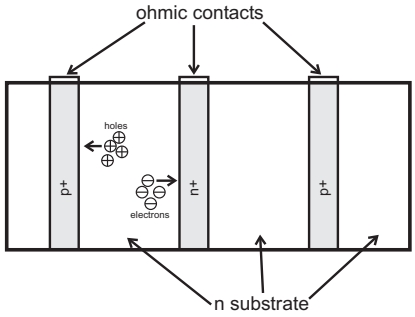

Figure 3.4: Transversal view of a 3-D detector.

The main advantage of this type of detectors is that the depletion region does not have to extend over the full thickness of the wafer, but only between two adjacent vertical diodes. This means that the applied bias voltage can be much smaller than needed for a conventional planar pixel detector with the same detector thickness and also the detector can be made sensitive up to the active edge. Additionally, the signals corresponding to both electrons and holes for each pixel are available to the processing electronics and the charge collection times are shorter due to the small distance between the electrodes, reducing also charge sharing between adjacent pixels.

3.7 Photon counting hybrid pixel detectors

In the mid-1970's, infrared focal plane arrays (IRFPAs) began to be developed for infrared imaging in military and astronomical applications [37, 38]. A typical IRFPA consists of a detector array fabricated with a narrow bandgap semiconductor (nominal bandgap values of 0.25 eV to 0.1 eV) connected to a so-called

silicon multiplexer. In its simplest form, the multiplexer functions as an array of switches connecting the detector pixel to an external preamplifier and pulse processing circuit. The detector and the multiplexer can be located on the same substrate (monolithic IRFPA), in different substrates connected via wire-bonds (pseudo-monolithic IRFPA) or in different substrates and connected using flip-chip or *Z-technology* methods (hybrid IRFPA).

The development of hybrid pixel detectors for high energy physics experiments began in the late 1980s at CERN* following the work done with IRFPAs. The first readout chip for hybrid pixel detectors was developed in the framework of the CERN-LAA detector R&D program in 1988. A small prototype array of pixel elements with 10 MHz synchronous binary readout circuits [40] proved the feasibility of these type of detector systems. The RD19 development program was then started at CERN to develop pixel detectors suited for the LHC experiments. The successors of the LAA chip were the OmegaD [41], the Omega2 [42] and the Omega3 [43].

In the following subsections we will concentrate on two readout chips for photon counting hybrid pixel detectors fabricated as a result of the efforts of the Medipix collaboration [44]. These are by no means the only devices of this type being developed in the world, and more information on other hybrid pixel detector systems can be found in e.g. [45, 46, 47, 48, 49].

3.7.1 The Medipix1 readout chip

The first Photon Counting pixel readout Chip (PCC) [50, 51, 52], also known as Medipix1, was developed using building blocks of the Omega3 chip, but with pixel shape and readout architecture adapted for imaging applications. Figure 3.5 shows an image taken with a Medipix1 readout chip connected to a silicon sensor [53].

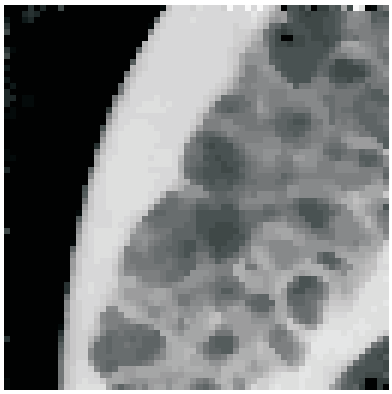

Figure 3.5: X-ray image of a sheep's spine taken with a Medipix1 readout chip connected to a silicon sensor.

The Medipix1 readout chip was designed and fabricated in a 1 μm CMOS technology and is composed of an array of 64 by 64 pixels. An additional row of dummy cells is used to sense the detector leakage current which is subtracted

*A much more comprehensive review of this work is offered in [39].

from the inputs of the sensitive cells. Each sensor element is connected to its corresponding readout electronics pixel via a bump-bond.

The Medipix1 chip was originally designed to be used with silicon sensors used in high energy physics experiments. These sensors are usually $p+$ implants on an n substrate material, and therefore the signal processing electronics were designed for hole collection.

Table 3.1 summarizes the most important characteristics of the Medipix1 chip and figure 3.6 shows a schematic drawing of the electronics included in each pixel of a Medipix1 chip.

Table 3.1: Characteristics of the Medipix1 chip

Pixel size	170 μm by 170 μm
Number of pixels	64 by 64
Chip sensitive area	10.88 mm by 10.88 mm
Maximum pixel counting rate	2 MHz
Minimum threshold	1400 electrons
Threshold spread (not adjusted)	350 electrons
Threshold spread (adjusted)	80 electrons
Maximum input signal	80000 electrons
Mean total noise level (without sensor)	130 electrons
Mean total noise level (with sensor)	140 electrons [54]
Counter depth	15 bits

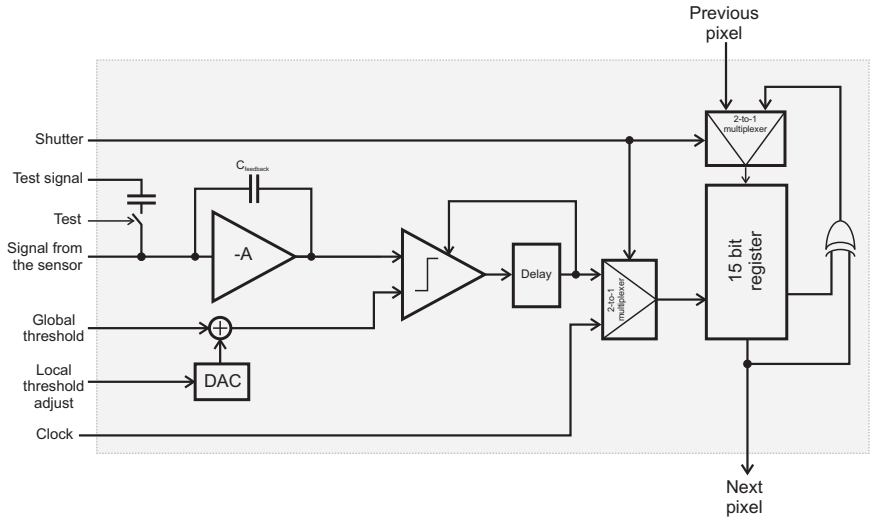

Figure 3.6: Block diagram of a pixel in the Medipix1 readout chip.

The signal generated in the sensor by the photon interaction is integrated and the resulting value is one of the inputs to a latched comparator. The other input is a programmable threshold, common to all pixels, which can be set corresponding to different values of deposited charge. Threshold uniformity

over the pixel matrix is improved through the availability of a 3-bit DAC per pixel. This DAC adds a small offset to the threshold in order to improve the threshold uniformity across the matrix. A short delay line which feeds back to the comparator is used to produce a pulse.

The *Shutter* signal shown in the figure is used to select the mode of operation for the pixels: image acquisition or digital data readout. In the image acquisition mode, the pulse from the delay line is used to clock a 15-bit shift register connected as a pseudo-random counter. The pixel can also be *masked* so that it is not active (e.g. for defective pixels).

All the status bits such as the mask bit, the threshold compensation, the test bit etc. are stored in a status register not shown in the figure. This register is loaded via the shift register.

The pseudo-random counter consists of a conventional shift-register with an XOR logic gate providing a feedback path. When the counter is clocked, the resulting binary sequence is pseudo-random in nature and repeats every $2^N - 1$ clock cycles (with N the length of the register). Compared to a conventional synchronous counter the pseudo-random counter is extremely simple, occupies a much smaller area and can therefore be implemented in a small pixel. In the readout mode, the register works as a conventional shift register and an external clock can be used to shift out the contents of the counter serially. The values of the pixel counters can then be read by an external data acquisition system [55]. Dedicated software or hardware must decode the pseudo-random counter values to obtain the true number of counts.

3.7.2 The Medipix2 readout chip

The second generation of the Medipix photon counting chip (Medipix2) was designed and fabricated in a 0.25 μm CMOS technology [56, 61]. Table 3.2 summarizes the main characteristics of the Medipix2 readout chip.

Table 3.2: Characteristics of the Medipix2 chip

Pixel size	55 μm by 55 μm
Number of pixels	256 by 256
Total chip area	16.12 mm by 14.11 mm
Chip sensitive area	14.08 mm by 14.08 mm
Maximum pixel counting rate	1 MHz
Minimum threshold	976 electrons
Threshold spread	138 electrons
Mean total noise level	190 electrons
Counter depth	13 bits plus overflow detection

With respect to the Medipix1 chip, some new features are included in the pixel cell such as leakage current compensation in each pixel, sensitivity to both electrons and holes (a.k.a. polarity selection); and an "energy-windowed" discriminator. The contents of the pixel counters can be read by the data acquisition system using a serial LVDS link [57] or a 32-bit wide parallel bus [58].

Figure 3.7 shows an image taken with a Medipix2 readout chip connected

to a silicon sensor. The chip has been successfully bonded to sensors based on different semiconducting materials [59, 60]

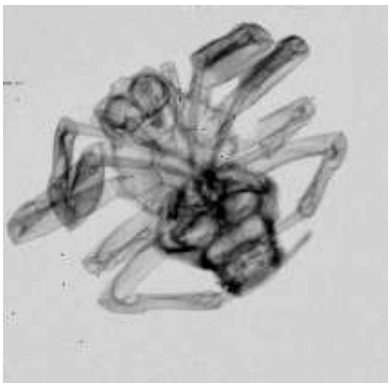

Figure 3.7: X-ray image of a spider taken with a Medipix2 readout chip bump-bonded to a silicon sensor. This image was taken at CERN by Lukas Tlustos.

More information with regards to the design and evaluation of the Medipix chips can be found in [61].

3.8 Summary

This chapter has shown that the result of a photon interaction in a semiconducting material is a number of free electrons and holes proportional to the energy deposited by the incident photon. In order to collect this charge, two contacts can be added to the detector and an electric field applied between them. To reduce the resulting DC current between the electrodes, rectifying contacts are used, especially reverse-biased pn junctions. The energy resolution of the detector is determined by the charge generation and collection mechanisms as well as by the noise added by the processing electronics.

To create a two-dimensional image of the incident radiation, position sensitive detectors such as microstrip, pad or pixel detectors are used. One of the most interesting of these is hybrid active pixel detectors, where the sensor and the processing electronics cells are fabricated separately and joined together using flip-chip techniques. Hybrid pixel detectors have been used successfully as photon counting imaging systems and are showing great potential in many different applications.

Bibliography

[1] S.M. Sze. *Semiconductor devices physics and technology.* John Wiley and sons, 2002.

[2] H. Spieler *Semiconductor detector systems.* Oxford University Press, 2005.

[3] C. Klein. Bandgap dependence and related features of radiation ionization energies in semiconductors. *Journal of applied physics*, 39(4):2029–2038, 1968.

[4] C. Klein. Semiconductor particle detectors: a reassessment of the Fano factor situation. *IEEE Transactions on Nuclear Science*, 15:214–226, 1968.

[5] U. Fano. On the theory of ionization yield of radiations in different substances. *Physics Review*, 70:44–52, 1946.

[6] T.E. Schlesinger and R.B. James. *Semiconductors for room temperature nuclear detector applications*. Academic Press, 1995.

[7] D.S. McGregor and H. Hermon. Room-temperature compound semiconductor radiation detectors. *Nuclear Instruments and Methods in Physics Research Section A*, 395(1):101–124, 1997.

[8] J. Darmo et al. The semi-insulating GaAs-based particle detector at IEE SAS: first imaging results. *Nuclear Instruments and Methods in Physics Research Section A*, 458(1-2):418–421, 2001.

[9] R.L. Bates et al. Development of low-pressure vapour-phase epitaxial GaAs for medical imaging. *Nuclear Instruments and Methods in Physics Research Section A*, 434(1):1–13, 1999.

[10] Y. Eisen et al. CdTe and CdZnTe gamma ray detectors for medical and industrial imaging systems. *Nuclear Instruments and Methods in Physics Research Section A*, 428(1):158–170, 1999.

[11] G. Bertuccio and R. Casiraghi. Study of Silicon Carbide for X-Ray Detection and Spectroscopy. *IEEE Transactions on Nuclear Science*, 50(1):175–185, 2003.

[12] K. Hitomi et al. Recent progress in thallium bromide detectors for X- and gamma-ray spectroscopy. *Nuclear Instruments and Methods in Physics Research Section A*, 458(1-2):365–369, 2001.

[13] P.G Pelfer et al. Present status and perspectives of the radiation detectors based on InP materials. *Nuclear Instruments and Methods in Physics Research Section A*, 458(1-2):400–405, 2001.

[14] L. van den Berg et al. Fabrication of HgI_2 radiation detectors. *Nuclear Instruments and Methods in Physics Research Section A*, 458(1-2):148–151, 2001.

[15] K.S. Shah et al. X-ray imaging with PbI_2-based a-Si:H flat panel detectors. *Nuclear Instruments and Methods in Physics Research Section A*, 458(1-2):140–147, 2001.

[16] E.H.M. Heijne et al. A silicon surface barrier microstrip detector designed for high energy physics. *Nuclear Instruments and Methods in Physics Research Section A*, 178:331–343, 1980.

[17] B.S. Avset et al. A new microstrip detector with double-sided readout. *IEEE Transactions on Nuclear Science*, 37(3):1153–1161, June 1990.

[18] F. Arfelli et al. A multilayer edge-on silicon microstrip single photon counting detector for digital mammography. *Nuclear Physics B (Proc. Supl.)*, 78:592–597, 1999.

[19] T. Mali et al. Silicon microstrip detectors for digital mammography: evaluation and spatial resolution study. *Nuclear Instruments and Methods in Physics Research Section A*, 460:76–80, 2001.

[20] M. Lundqvist et al. Evaluation of a Photon-Counting X-Ray Imaging System. *IEEE Transactions on Nuclear Science*, 48(4):1530–1536, 2001.

[21] E. Gatti and P. Rehak. Semiconductor Drift Chamber - an Application of a Novel Charge Transport Scheme. *Nuclear Instruments and Methods in Physics Research Section A*, 225:608–614, 1984.

[22] A. Castoldi et al. The controlled-drift detector. *Nuclear Instruments and Methods in Physics Research Section A*, 439(2-3):519–528, 2000.

[23] S.O. Kasap and J.A. Rowlands. Direct-Conversion Flat-Panel X-Ray Image Sensors for Digital Radiography. *Proceedings of the IEEE*, 90(4):591–604, April 2002.

[24] L. Strüder et al. A 36 cm^2 large monolythic pn-charge coupled device X-ray detector for the European XMM satellite mission. *Review of Scientific Instruments*, 68(11):4271–4274, November 1997.

[25] T.O. Tümer et al. Hybrid Direct Conversion Detectors for Digital Mammography. *IEEE Transactions on Nuclear Science*, 46(6):2093–2097, December 1999.

[26] T.O. Tümer et al. High-resolution pixel detectors for second generation digital mammography. *Nuclear Instruments and Methods in Physics Research Section A*, 497(1):21–29, 2003.

[27] P. Fischer et al. First operation of a pixel imaging matrix based on DEPFET pixels. *Nuclear Instruments and Methods in Physics Research Section A*, 451:651–656, 2000.

[28] R.H. Richter et al. Design and technology of DEPFET pixel sensors for linear collider applications. *Nuclear Instruments and Methods in Physics Research Section A*, 511:250–256, 2003.

[29] W. Chen et al. Active pixel sensors on high-resistivity silicon and their readout. *IEEE Transactions on Nuclear Science*, 49(3):1006–1011, June 2002.

[30] F.X. Pengg. *Monolithic Silicon Pixel Detectors in SOI technology.* PhD thesis, CERN, January 1996.

[31] M. Amati et al. Hybrid active pixel sensors and SOI inspired option. *Nuclear Instruments and Methods in Physics Research Section A*, 511(1-2):265–270, 2003.

[32] M. Lozano et al. Bump bonding of pixel systems. *Nuclear Instruments and Methods in Physics Research Section A*, 473(1-2):95–101, 2001.

[33] Ch. Grah. Pixel detector modules using MCM-D technology. *Nuclear Instruments and Methods in Physics Research Section A*, 465(1):211–218, 2001.

[34] K. Spartiotis et al. A directly converting high-resolution intra-oral X-ray imaging sensor. *Nuclear Instruments and Methods in Physics Research Section A*, 501(2-3):594–601, 2003.

[35] S.I. Parker et al. 3D - A proposed new architecture for solid-state radiation detectors. *Nuclear Instruments and Methods in Physics Research Section A*, 395(3):328–343, 1997.

[36] V. Wright et al. A new dimension to semiconductor detectors in high-energy physics and medical imaging. *Nuclear Instruments and Methods in Physics Research Section A*, 513(1-2):345–349, 2003.

[37] D.A. Scribner et al. Infrared focal plane array technology. *Proceedings of the IEEE*, 79(1):66–85, January 1991.

[38] C.-C. Hsieh et al. Focal-Plane-Arrays and CMOS Readout Techniques of Infrared Imaging Systems. *IEEE Transactions On Circuits And Systems For Video Technology*, 7(4):594–605, August 1997.

[39] E.H.M. Heijne. Semiconductor micropattern pixel detectors: a review of the beginnings. *Nuclear Instruments and Methods in Physics Research Section A*, 465(1):1–26, 2001.

[40] M. Campbell et al. A 10 MHz micropower CMOS front end for direct readout of pixel detectors. *Nuclear Instruments and Methods in Physics Research Section A*, 290:149–157, 1990.

[41] F. Anghinolfi et al. A 1006 element hybrid silicon pixel detector with strobed binary output. *IEEE Transactions on Nuclear Science*, 39(4):654–661, 1992.

[42] M. Campbell et al. Development of a pixel readout chip compatible with large area coverage. *Nuclear Instruments and Methods in Physics Research Section A*, 342:52–58, 1994.

[43] E.H.M. Heijne et al. LHC1: a semiconductor pixel detector readout chip with internal, tunable delay providing a binary pattern of selected events. *Nuclear Instruments and Methods in Physics Research Section A*, 383(1):55–63, 1996.

[44] http://www.cern.ch/medipix/.

[45] B. Mikulec. Development of segmented semiconductor arrays for quantum imaging. *Nuclear Instruments and Methods in Physics Research Section A*, 510(1-2):1–23, 2003.

[46] P. Seller et al. Photon counting hybrid pixel detector for X-ray imaging. *Nuclear Instruments and Methods in Physics Research Section A*, 455(3):715–720, 2000.

[47] M. Lindner et al. Comparison of hybrid pixel detectors with Si and GaAs sensors. *Nuclear Instruments and Methods in Physics Research Section A*, 466(1):63–73, 2001.

[48] P. Delpierre et al. Large Surface X-Ray Pixel Detector. *IEEE Transactions on Nuclear Science*, 49(4):1709–1711, August 2002.

[49] E.F. Eikenberry et al. PILATUS: a two-dimensional X-ray detector for macromolecular crystallography. *Nuclear Instruments and Methods in Physics Research Section A*, 501(1):260–266, 2003.

[50] M. Campbell et al. Readout for a 64 x 64 pixel matrix with 15-bit single photon counting. *IEEE Transactions on Nuclear Science*, 45(3):751–753, 1998.

[51] M.G. Bisogni et al. Performance of a 4096 pixel photon counting chip. *Proceedings of the SPIE*, 3446:298–304, 1998.

[52] C. Schwarz et al. Measurements with Si and GaAs pixel detectors bonded to photon counting readout chips. *Nuclear Instruments and Methods in Physics Research Section A*, 466(1):87–94, 2001.

[53] J.-P. Girardeu-Montaut et al. Table-top laser-driven ultrashort electron and X-ray source: the CIBER-X source project. *Nuclear Instruments and Methods in Physics Research Section A*, 452(1-2):361–370, 2000.

[54] A. Fornaini et al. Soft X-ray sensitivity of a photon-counting hybrid pixel detector with a silicon sensor matrix. *Nuclear Instruments and Methods in Physics Research Section A*, 466(1):142–145, 2001.

[55] G. Bardelloni et al. A new read-out system for an imaging pixel detector. In *Proceedings of the IEEE Nuclear Science Symposium and Medical Imaging Conference, Lyon, France, October 15-20, 2000*, pages 57–60.

[56] X. Llopart et al. Medipix2, a 64k pixel read out chip with 55 μm square elements working in single photon counting mode. *IEEE Transactions on Nuclear Science*, 49(5):2279–2283, October 2002.

[57] D. San Segundo Bello et al. An interface board for the control and data acquisition of the Medipix2 chip. *Nuclear Instruments and Methods in Physics Research Section A*, 509(1-3):164–170, 2003.

[58] V. Fanti et al. Medipix2 parallel readout system. *Nuclear Instruments and Methods in Physics Research Section A*, 509(1-3):171–175, 2003.

[59] G. Mettivier et al. First images of a digital autoradiography system based on a Medipix2 hybrid silicon pixel detector. *Physics in Medicine and Biology*, 48:173–181, 2003.

[60] M. Chmeissani et al. Charge Sharing Measurements of pixilated CdTe using Medipix-II chip. In *Proceedings of the 21st IEEE Instrumentation and Measurement Techniques Conference, Como, Italy, 18-20 May 2004*, pages 787–791.

[61] Llopart Cudie, X and Frojdh, C and Campbell, M. *Design and Characterization of 64K Pixels Chips Working in Single Photon Processing Mode.* PhD thesis, Mid Sweden Univ., Sundsvall, 2007. Presented on 25 May 2007.

Chapter 4

System definition

Under most circumstances, the charge deposited by a photon after an interaction is proportional to the energy it lost in the interaction. A system can be built which performs a measurement of the energy lost by the photon. Such a system must detect each photon interaction in a certain area of the sensor material (pixel) and measure the charge deposited by this photon in that area.

As explained earlier in section 2.6, radiation imaging systems can be divided into *integrating* and *quantum imaging* systems. Integrating systems measure the charge accumulated in a certain area of the detector as a result of the interaction of photons with the detecting material. Quantum imaging systems, on the other hand, are able to process each individual photon interaction [1, 2, 3, 4, 5, 6]. Almost all of the currently existing quantum imaging systems are *photon counting*. They count the number of photons that hit a certain area of the detector material (a pixel) during a certain time window. If the energy lost in each photon interaction is measured, one can speak of a *spectroscopic quantum imaging system*. Spectroscopic quantum imaging systems can be used, for example, to resolve the *K-edge* discontinuities* of different chemical elements in order to identify them [7].

As more and more transistors are available in the same area one can think of building a spectroscopic quantum imaging system by putting one ADC in each pixel. More processing tasks can be carried out locally in the pixel, ultimately leading to a *programmable digital pixel* [8] which can perform complex signal processing tasks in the digital domain, reducing the data throughput and/or increasing the image quality. Additionally, higher signal-to-noise ratio (SNR) and lower power consumption should be possible by having the converter placed as close as possible to the sensor interface.

This thesis describes a spectroscopic quantum imaging system designed with an ADC in each pixel. In particular, it describes the electronics used in a hybrid semiconductor pixel detector. This chapter will present the different parts of the system. Section 4.1 gives an overview of the different parts that make up the system. Section 4.2 introduces in a bit more detail the different circuits needed, starting with the circuits found in the pixels (section 4.2.1), continuing with the architecture and organization of the pixels in the array (section 4.2.2) and ending with the circuits found outside of the pixel array (section 4.2.3). Section 4.3

*Also known as *k fluorescence lines*. See section 2.4.5.

presents some considerations regarding design for test. This topic is discussed in more detail in appendix B. Finally, section 4.4 offers some conclusions.

4.1 System overview

The basic building blocks of a radiation imaging system are the radiation source, the detector (which includes the sensor and the processing electronics) and finally the control and data acquisition system. Figure 4.1 shows a block diagram of a typical radiation imaging system.

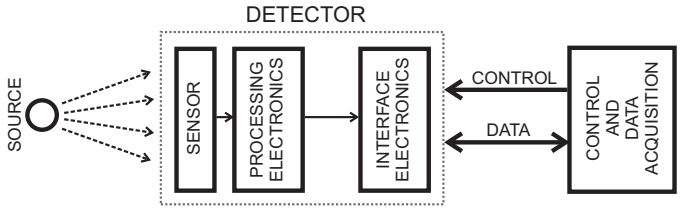

Figure 4.1: Block diagram of typical radiation imaging system.

In many cases, and in particular in industrial and biomedical imaging applications, the radiation source can be chosen or adapted to fit the characteristics of the application. Under these circumstances, a spectroscopic imaging system can be built using one or more mono-energetic radiation sources. One separate image is obtained for each energy using conventional imaging systems [9] and the different images are later combined to form the final image. In most cases, though, the radiation source has a more or less broad energy spectrum or is external to the system (e.g. in the case of X-ray and gamma-ray astronomy). The spectrum of these radiation sources could also be filtered before it arrives at the detector, and different images could then be taken, each one with a different filter [10]. However, common filtering techniques used with visible light cannot be used at high photon energies, and much more complex (and expensive) filtering methods are needed.

If a solid-state sensor is being used, one can use the energy dependence of the attenuation length of the photons in the material, or build the sensor with layers of different materials. An estimation can then be made of the energy deposited by the photon in the sensor by processing the signal depending on the position within the sensor where the interaction has taken place [11], similar to the way it is done in some visible light imaging sensors[12, 13].

A more general approach to building a spectroscopic quantum imaging system is to process electronically the signal produced by the interaction of the photon in the sensor. This approach relaxes the specifications of the radiation source and the sensor. One possibility to build such a system extends the photon counting approach described in section 3.7 and uses more than one set of comparators and counters [14]. A second, more general approach processes every photon interaction independently in each pixel, for example by using pixel-level analog-to-digital converters (ADCs).

4.1.1 The radiation source

The source indicated in Figure 4.1 includes the radiation source itself and, depending on the type of application, the object being imaged. The goal of the system is to detect the photons directly emitted by a source, absorbed by an object or reflected in an object. The nature of the source and the object will determine the maximum and minimum photon energy to be detected by the system. Depending on the ionization energy of the sensor material, these numbers will give the minimum and maximum charge that needs to be detected by the processing electronics, setting the specification for signal-to-noise ratio. The source will also fix the maximum photon rate that needs to be handled by the processing and interface electronics. The specifications chosen for the system presented in this thesis are summarized in table 4.1. These values are chosen more or less arbitrarily but fit most X-ray (and low-energy gamma-ray) imaging applications*.

Table 4.1: Source specifications.

Name	Value	Unit
Minimum photon energy	5	keV
Maximum photon energy	100	keV
Photon rate	10^6	photons/second/mm^2

4.1.2 The detector subsystem

The *detector* subsystem comprises the *sensor*, the *processing electronics* and the *interface electronics*. These three elements can be physically located in the same chip. Nevertheless, currently the sensor and the electronics are fabricated separately for maximum efficiency and then connected using flip-chip (or similar) bonding techniques. Eventually, separate chips could be used for the pixel processing electronics and for the interface and peripheral electronics, using one of the various existing three-dimensional integration techniques [15, 16, 17, 18, 19] to put the various elements together.

The *sensor* is manufactured in a semiconducting material. The most typically used materials for pixel detectors nowadays are silicon (Si), gallium arsenide (GaAs) and cadmium telluride (Cd(Zn)Te) [20, 21]. As explained in section 3.3, the charge generated in the sensor by a photon of a certain energy depends on the material and, in particular, on its *ionization energy*. In general, silicon is used as much as possible due to the matureness of its manufacturing process, as well as the purity of the material. However, for energies above a few tens of keV, the photons are not fully stopped in silicon unless very thick detectors are used. For these higher energies, materials with higher atomic number such as the above mentioned GaAs and CdTe are used.

The *processing electronics* take the signal generated in the sensor and extract a measure of the charge resulting from the photon interaction.

The function of the *interface electronics* is to read the output of the pixel

*The lower value of 5 keV is close to the emission line of ^{55}Fe. The maximum number covers high energy X-rays as well as gamma radiation. The photon rate is typical for emission radiography.

processing electronics and format it before sending it to the *control and data acquisition system*. The specifications for this part of the system arise from the data rate needed for reading the pixel data for the specified photon rate. As such, this specification is a function of the number of pixels and the coding of the pixel data.

One specification that has not been addressed in this thesis and which would follow from the application is the *radiation hardness* of the electronics. This turns out not to be a major issue for the basic specifications of the system. In cases where the photon flux is larger or the maximum energy is higher, it is needed to evaluate the need for radiation hardness measures. In that case, manufacturing technologies different from standard CMOS[22] or a different design methodology[24, 23, 25] should be used.

4.1.3 The control and data acquisition system

The *control and data acquisition* system serves as an interface between the detector subsystem and the final display/storage unit. An example of a control and data acquisition system using a serial interface was designed and built by the author of this thesis for the Medipix2 chip in parallel to the work described in this thesis [26].

4.2 The processing and interface electronics

Figure 4.2 shows a block diagram of a readout chip for a hybrid pixel detector. The processing electronics are located in the pixels of the pixel array. The interface electronics can be divided between the pixel readout electronics and the off-chip interface electronics, represented by the *DATA TX* and *DATA RX* blocks.

Additional support circuits such as generation of bias voltages and currents for the operation of the pixels and control of the operation of the pixels (masking, calibration, etc...) are typically located in the periphery of the pixel array.

Section 4.2.1 introduces the circuitry located in the pixels, with an explanation of why it was chosen to design the system with an ADC in every pixel in subsection 4.2.1.1. The architecture of the pixel array or, in other words, the organization of the pixels and how they are connected to the peripheral electronics, is explained in section 4.2.2. Finally, section 4.2.3 introduces the peripheral electronics.

4.2.1 Pixel electronics

The circuits located in the pixels will process the signal from the sensor and interact with the circuitry located in the periphery of the chip (or in a separate chip) to read the data from the pixels.

Figure 4.3 shows a block diagram of the different functional blocks present in one pixel of the system described in this thesis: the *front-end*, the *analog-to-digital converter (ADC)*, the *readout block* and a *pixel configuration block*.

The *front-end* circuitry performs the necessary analog pre-processing prior to the analog-to-digital conversion. First, it integrates the current pulse from the detector. The result of the integration is then held constant for a short time

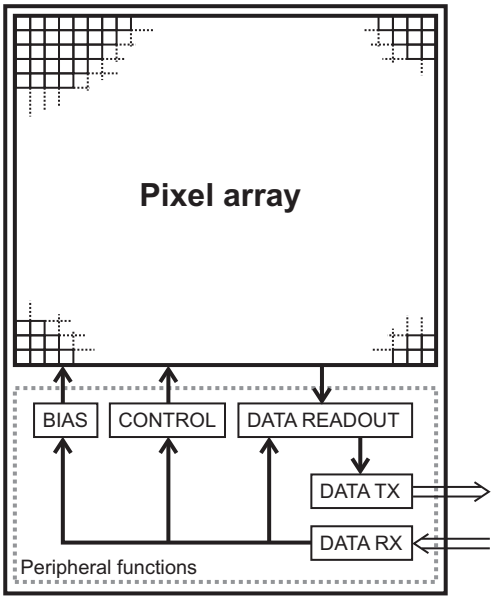

Figure 4.2: Block diagram of the electronics for a radiation imaging pixel detector.

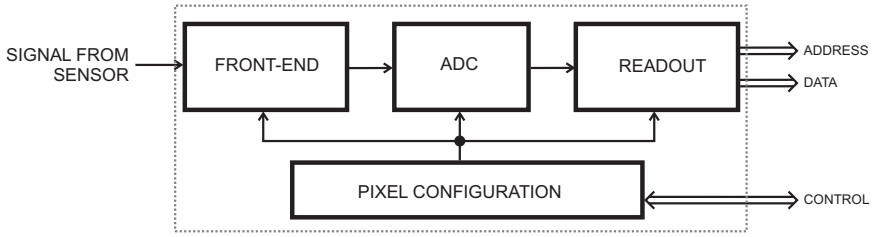

Figure 4.3: Block diagram of the pixel electronics.

so that the ADC can perform the conversion*. It also detects the occurrence of the photon hit to notify the ADC that it can perform the conversion. All these functions are explained in more detail in chapter 5.

When the front-end electronics report the occurrence of a photon hit, the *analog-to-digital converter* converts the result of the integration in the front-end electronics. A detailed analysis of this block can be found in chapter 6.

The digital output of the ADC, as well as the position of the pixel in the imaging array are read from the pixel by the *digital data readout* subsystem, which involves circuitry in the periphery of the chip as well as the *readout* block in the pixels.

The *pixel configuration* block is used to configure the operation of the pixel: to test the operation of one or all the functional blocks, to bypass or turn off the pixel if it is found not to work correctly, to make local threshold adjustments at the pixel level, etc. It can be implemented as a digital register, and the registers in the pixel array can be set in a similar way as it is done, for example, in the Medipix family of photon counting chips [27, 1].

Other functions that can be added to the pixel electronics but that are not addressed in this work are: in-pixel memory, parallel analog processing or recording the time at which the photon interaction took place. If the data corresponding to a photon interaction has not been read from the pixel at the time that another photon interaction happens, the information corresponding to the second interaction will be lost, degrading the efficiency of the system. To prevent this, local memory can be implemented in the pixel (e.g. a FIFO after the ADC). Another possibility would be parallel analog processing, e.g. having two ADCs in the pixel and using one or the other alternatively. It could also be interesting to add the information on when the photon interaction took place to the data read from the pixel[28]. This *timing information* could be captured using the signal indicating that a photon interaction has been detected and a timing reference distributed to the pixels. If this time stamp is recorded in digital form it can be read from the pixel using the same architecture described later in section 4.2.2. Overall, the complexity of the system will increase due to the need of distributing a global time reference to the pixels, as well as the increase in data bits to be transferred per interaction for each pixel. Although this feature has not been considered in this thesis, the system described can also be used to capture moving images. The precise timing information of the photon interaction is not available, but a coarse timing information, related to the readout time of the pixels is inherently attached to the information read from the pixels.

At this point, the main specifications for the pixel electronics that can be fixed are the pixel area, the power consumption and the photon processing time. The pixel area is directly related to the image resolution and thus, in principle the pixels should be as small as possible. Nevertheless, there are several limiting factors such as the current state of flip chip interconnect technologies and the charge spread in the sensor which limit the minimum useful pixel area. In that respect, and remembering that there is no given specification for this system, we chose a pixel area slightly larger than current state of the art (the 55 μm x 55 μm of the Medipix2 chip [1]) to allow the inclusion of the new circuitry

*Note that the *sample-and-hold* function is included in the front-end electronics and not in the ADC itself.

(ADC and readout). The chosen goal for pixel area is of 100 μm x 100 μm. In terms of power consumption, a somehow arbitrary choice had to be made. Based on the nature of our system and on current existing quantum imaging systems, a value of 1 W per chip* was chosen. For a 1 cm^2 imaging area in the chip and 100 μm x 100 μm pixels, it leads to approximately 100 μWatt per pixel. The photon processing time corresponds to the time it takes to process a photon interaction, from the photon hitting the detector to the digital data being read. With the photon rate specified in table 4.1 and assuming pixels of 100 μm x 100 μm, the maximum photon processing time is 10 μs. This time has to be spread between the front-end processing, the ADC conversion time and the time it takes to read the data from the pixel.

Figures 4.4 and 4.5 show the layout and photograph of the pixel used in the pixADC4 test-chip. This pixel does not include the configuration block.

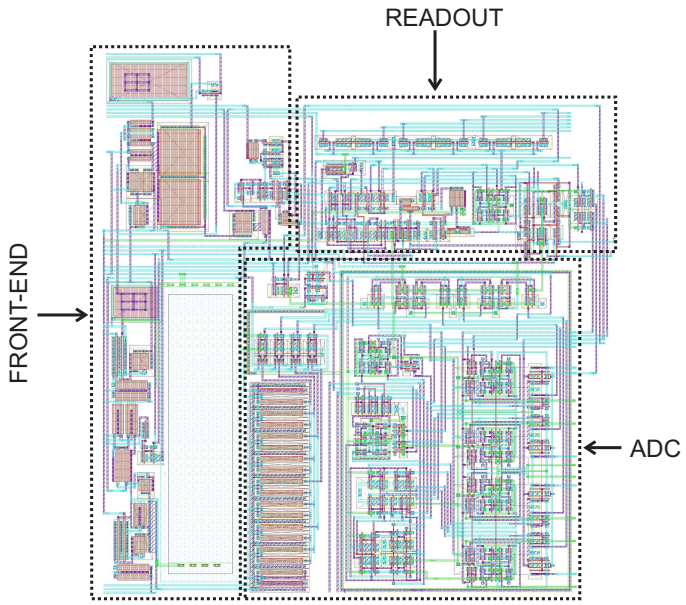

Figure 4.4: Layout of a pixel in the pixADC4 prototype chip.

4.2.1.1 Pixel-level analog-to-digital converters

The energy information can be read from the pixels in analog form [29, 30], but crosstalk as well as limitations in the on-chip interconnections would lead to complex readout schemes in order to maintain a reasonable speed and signal-to-noise ratio. Analog-to-digital converters (ADC) are then used in out system to convert the (analog) energy information to a digital representation.

Research on ADCs for imaging devices has been going on for some years in the field of infrared and visible-light CMOS imaging systems [31, 8]. Originally,

*This number is assumed to correspond to the pixels only, i.e. it excludes the power consumption in the periphery (biasing, communication, etc...).

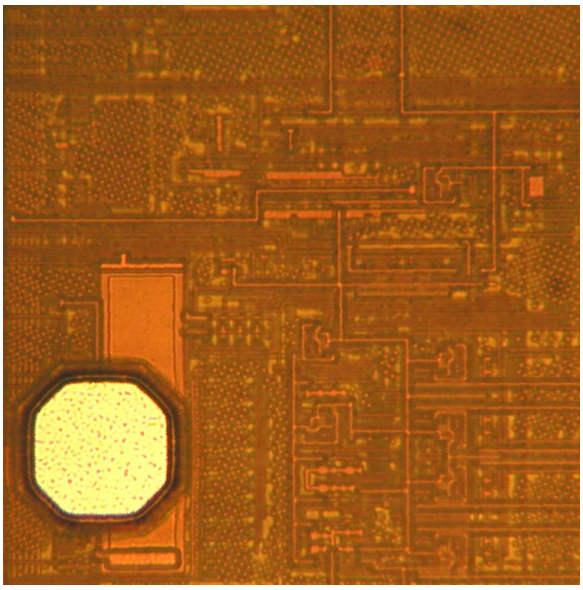

Figure 4.5: Photograph of one pixel in the pixADC4 prototype chip. The bump-bond opening is clearly visible.

one ADC was used to process the information from all the pixels in the chip [32, 33, 34]. In an integrating imaging system there is a clear separation between the time used to collect the charge resulting from the photon interactions and the time when this accumulated charge is read from the pixels and processed. This feature is exploited in both column-level [35, 36] and pixel-level [37, 38, 39, 40, 41, 42, 43] ADCs to operate, respectively, all columns or all pixels in parallel. As a result, slower ADCs than those in the chip-level approach can be used.

In a quantum imaging system one can also think of sharing one ADC by several pixels (e.g. one ADC per chip, one ADC per column or one ADC per N pixels). This approach offers in principle several advantages. For example, smaller pixels can be used while, at the same time the ADC can occupy a larger area or consume more power than in the case of pixel-level ADCs. However, chip-level or column-level ADC approaches are basically equivalent to reading the data in analog form and thus suffer from the same problems. To solve these problems the ADCs should be located in the pixel array. If an ADC is shared by several pixels, the distribution in the layout of the pixels and the ADC make the connection between the pixels in the sensor and the readout electronics more complex. Additionally, the readout speed from the ADC to the periphery of the chip and the speed of the ADC itself must increase by a number equal to the number of pixels that share the ADC. These disadvantages lead us to investigate the approach of using one ADC in each pixel. In any case, whether one uses one ADC for several pixels or one ADC per pixel, the same readout principle explained in section 4.2.2 can be used with small modifications for each particular case.

Hybrid detectors with analog-to-digital conversion at the pixel level are used

in high energy physics experiments. For example, the FPIX chip [44] to be used in the BTeV experiment in Fermilab uses a 3-bit flash ADC, and the readout chip for the pixel detector in the ATLAS Experiment [45] at CERN uses the *Time Over Threshold* technique [46] to determine the deposited energy. However, the application as well as the architecture of these chips are very different from the spectroscopic quantum imaging system described in this thesis.

4.2.2 Array architecture

In currently existing readout chips for photon counting pixel detectors there are two clearly separated time periods [2]. In the first period the image is being acquired and the pixel counters are counting. In the second period the contents of the counters are read and the counters are connected as shift registers*. When each photon interaction has to be processed independently this separation does not exist anymore at the chip or system level, but only at the pixel level.

Once a photon interaction has been processed, the output of the pixel processing electronics and the position of the pixel in the array must be read from the pixel in order to allow the pixel to process a new photon interaction. Alternatively, this data can be stored in the pixel for later readout, but this approach should only be used once the application where the system will be used is known. In our study we will assume that the data must be read immediately after being processed, as this will give the ultimate limit in the readout speed.

The selection of the pixel to be read can be done in two ways: either externally by providing the row and column address of the pixel, or the pixels themselves can trigger the readout sequence when they are hit by a photon. The system described in this thesis is *event-driven*. A pixel requests control of an internal data bus after having processed a photon interaction. When this control is granted, the pixel puts its position coordinates in the array (row and column), as well as the contents of the ADC in the bus. When the peripheral readout circuitry notifies the pixel that the data has been successfully read, the pixel is free to process a new photon interaction†.

The pixel array is organized as an asynchronous system. There is no clock signal being distributed to the pixels for the purpose of reading the pixel data. The advantages (and disadvantages) of using an asynchronous architecture have been discussed extensively in the last years as a result of new interest in asynchronous systems [49]. In the case of the system described in this thesis, the system is asynchronous in itself: the pixels are being hit by photons irrespective of any central timing reference. It is thus logical to try to exploit this characteristic when designing the data readout system.

Given the likelihood that more than one pixel requests control of the array-wide data bus, there must be an *arbitration* system to decide which pixel is going to be read. A *token bus*-like approach is used in the system described in this thesis ‡. A *token* is generated at a central point (e.g. in the peripheral

*One important exception to this is the XPAD chip[5]. In this chip, during image capture only the overflow of the pixel registers is read. That is, when the counter of one pixel is full, its address is read and not the pixel contents. This allows a high photon rate in the system for which the pixel was designed.

†Similar readout systems have been described in the literature [47, 48] for other pixel readout chips, but their approach was less general and more limited in their application.

‡In a token bus ring a token is passed around the network nodes and only the node possessing the token may transmit. If a node doesn't have anything to send, the token is

electronics) and circulates from pixel to pixel until it reaches back the starting point and starts circulating again. When a pixel that has processed a photon interaction receives the token, it stops the circulation of the token momentarily and takes full control of the common data bus, putting in the bus the result of the analog-to-digital conversion as well as its position (row and column) in the array.

4.2.2.1 Array organization

As will be explained later in chapter 7, the pixels are organized in groups of two columns. Figure 4.6 shows a block diagram of such a two-column block. A *column control and readout* circuit is located outside of the pixel array (e.g. in the periphery of the readout chip). It controls the token circulation and receives the pixel data (address and ADC data).

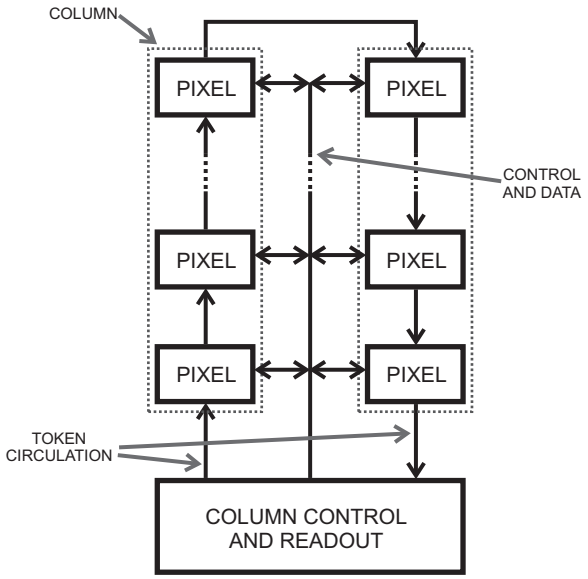

Figure 4.6: Block diagram of a two-column block.

The organization and interconnection of the different two-column blocks can be chosen in different ways: from having one link to the external control and data acquisition subsystem for each block to having one link for all the two-column blocks in one readout chip*. For simplicity, the latter option is the one studied in this work. In both cases (one link per two-column block or one link for all blocks) the interaction mechanism of each column block with the pixels in its corresponding columns will be the same.

passed on to the next node on the virtual ring.

*One can also think of intermediate solutions where several blocks share one link. The final decision on the implementation is imposed by the requirements of the application: the solution with one link per two-column block could allow a high data rate at the cost of a large number of connections between the readout chip and the control and data acquisition system, while the solution with one link for the whole chip simplifies the interface but limits somehow the maximum achievable data rate.

4.2.2.2 Pixel data readout

Once a pixel gains control of the data bus, the communication between the pixels and the column readout block has to be performed as fast as possible so that the pixel is free to process a new photon interaction. This *readout speed* will set the limit to the maximum photon rate that can be processed without losing efficiency. The distance from the pixels to the readout circuitry in the periphery will have a big influence on the readout speed. This distance can range from tens of micrometers to several millimeters for large imaging arrays. This means that the delay associated with the metal interconnections will be the limiting factor in the readout speed of the chips [50, 51]. Two different possibilities arise for the circuits that will be used: *voltage-mode* and *current-mode* signaling.

When using *voltage-mode* signaling the load capacitance (in our case the capacitance of the metal interconnections) must be charged (or discharged) by the transmitter circuit to a certain voltage level in a time as short as possible for the receiver circuitry to detect the binary information. The amount of current to be drawn from the power supplies to charge or discharge this load capacitance will increase with the value of the capacitance, the voltage level needed and the required charging time. Although the design of both the driver and the receiver circuitry for voltage mode signaling is simpler than for current mode signaling, the power consumption as well as the sizes of the transistors of the driver circuitry would be relatively large. If several of these drivers have to be implemented in each pixel (e.g. one for each bit of the ADC output word), the overall system efficiency will degrade *.

Current-mode signaling relies on the existence of a receiver circuit with very low (ideally zero) input impedance which senses the current and conveys it to a low capacitance node where the needed voltage level can be achieved fast and with a relatively low current drawn from the supply. This means that the driver does not have to charge the load (wiring) capacitance to a voltage level at a very fast speed and only needs to send the data as current. The disadvantage of this approach is that the design of the receiver circuitry is more complicated than in the case of *voltage-mode* signaling.

In order to minimize the effect of the distance from the pixels to the readout circuitry, the system described in this thesis uses *current-mode* signaling for all signals (data and control) going from the pixels to the periphery. For the signals being sent from the periphery to the pixels, conventional *voltage-mode* signaling was used. The use of *current-mode* signaling simplifies the pixel circuitry at the cost of adding complexity in the peripheral readout electronics for the detection of the signals from the pixels. This means that the pixel size and power consumption can be kept relatively small.

4.2.3 Peripheral electronics

Figure 4.7 shows a block diagram of the most important peripheral functions.

These functions can be located in one edge of the chip where the pixel array is found, or they can be part of a separate chip. This last possibility is made possible by recent advances in chip-to-chip interconnection technologies [15, 16, 17, 18, 19], and it allows large area coverage as well as more flexibility in

*If a serial readout were implemented the number of drivers is of course small, but at the cost of a longer readout time.

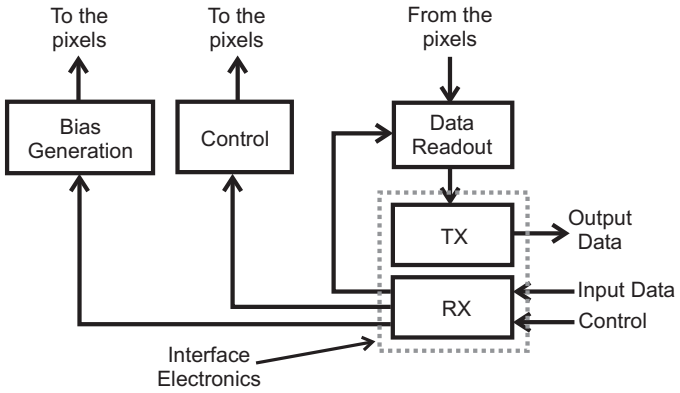

Figure 4.7: Block diagram of the basic circuitry in the periphery of an imaging pixel detector readout chip.

the design of the different components of the system (sensor, front-end analog processing electronics and digital readout electronics). Nevertheless, in this work the peripheral electronics are considered to be a part of the same chip where the pixel array is found and are located in one edge of the chip.

An example of bias circuitry for pixel detector readout chips is briefly considered in Appendix A. The circuitry in charge of the data readout was introduced earlier in section 4.2.2 and will be explained in more detail in chapter 7. The control block must take care that the *pixel configuration data* is delivered correctly to the pixels.

In order to interact with the control and data acquisition system, data communication blocks (i.e. at least one data transmitter and one data receiver) must be used. In the figure they are represented by the *RX* and *TX* blocks. The design of such blocks for the system presented in this work is beyond the scope of this thesis, and thus will not be addressed here. Work in this area was started already and is the subject of another PhD thesis [52, 53].

4.3 Design for test

A very relevant issue when building the final detector systems is the availability of so-called *known-good-dies*. The process of connecting the readout chip to the sensor element is expensive and usually not reversible. This means that the functionality of the readout chip must be verified before the further build-up of the hybrid system. For the same reason, it must be possible to monitor the performance of the different circuits which make up the readout chip.

To achieve all this, so-called *Design for test* (DfT) capabilities must be built into the system. Appendix B offers an explanation of how such measures would work in the system described in this thesis.

4.4 Summary and conclusions

This chapter started by explaining the different parts that make up a radiation imaging system and, in particular, a *spectroscopic quantum imaging system*.

Although this type of systems could be built using radiation with a well-known energy spectrum or sensors with well-known and controllable characteristics, an easiest and more cost-effective way is to use conventional radiation sources and sensor materials and do the work in the processing electronics. One processing method which takes advantage of the latest developments in microelectronics technology and design is based on processing the signal from the sensor by including an analog-to-digital converter (ADC) in each pixel.

In order to take full advantage of the use of the pixel-ADCs, care must be taken, not only in the design of the processing electronics prior to the ADC, but also in the architecture of the pixel array. Given the nature of the system, each photon interaction must be processed independently. This means that, for each interaction, the location of the pixel in the array where the interaction took place, as well as the output of the ADC must be available to the *control and data acquisition* subsystem as quick as possible. For this type of application, then, an asynchronous token bus architecture is used.

Bibliography

[1] X. Llopart et al. Medipix2, a 64k pixel read out chip with 55 μm square elements working in single photon counting mode. *IEEE Transactions on Nuclear Science*, 49(5):2279–2283, October 2002.

[2] B. Mikulec. Development of segmented semiconductor arrays for quantum imaging. *Nuclear Instruments and Methods in Physics Research Section A*, 510(1-2):1–23, 2003.

[3] P. Seller et al. Photon counting hybrid pixel detector for X-ray imaging. *Nuclear Instruments and Methods in Physics Research Section A*, 455(3):715–720, 2000.

[4] M. Lindner et al. Comparison of hybrid pixel detectors with Si and GaAs sensors. *Nuclear Instruments and Methods in Physics Research Section A*, 466(1):63–73, 2001.

[5] P. Delpierre et al. Large Surface X-Ray Pixel Detector. *IEEE Transactions on Nuclear Science*, 49(4):1709–1711, August 2002.

[6] E.F. Eikenberry et al. PILATUS: a two-dimensional X-ray detector for macromolecular crystallography. *Nuclear Instruments and Methods in Physics Research Section A*, 501(1):260–266, 2003.

[7] J. Giersch et al. The influence of energy weighting on X-ray imaging quality. *Nuclear Instruments and Methods in Physics Research Section A*, 531(1-2):68–74, 2004.

[8] A. El Gamal et al. Pixel Level Processing - Why, What, and How? *Proceedings of the SPIE*, 3650:2–15, 1999.

[9] G. Baldazzi et al. First Results with a Novel X-ray Source for Dual Energy Angiography. In *Proceedings of the IEEE Nuclear Science Symposium and Medical Imaging Conference, San Diego, November 4-10, 2001*, volume 3, pages 1615–1619.

[10] C. A. Mistretta and F. Kelcz. Differential X-ray method and apparatus. US Patent 3974386, 1976.

[11] E.H.M. Heijne. Spectroscopic imaging of X-rays: a new look. In *Proceedings of the IEEE Nuclear Science Symposium and Medical Imaging Conference, Portland, October 19-25, 2003*, volume 1, pages 228– 231.

[12] A. El Gamal. Trends in CMOS Image Sensor Technology and Design. In *Proceedings of the 2001 IEEE International Electron Devices Meeting (IEDM), Washington DC, 3-5 December 2001.*

[13] http://www.foveon.com.

[14] M. Clajus et al. Front-End Electronics for Spectroscopy Applications (FESA) IC. In *Proceedings of the IEEE Nuclear Science Symposium and Medical Imaging Conference, Lyon, October 15-20, 2000*, volume 2, pages 227–229.

[15] W. B. Hornback. Three dimensional sensor readout electronics using conventional detector hybrid assemblies. *Proceedings of the SPIE*, 2745:50–54, 1996.

[16] K. Tsubouchi et al. A new concept of 3-dimensional multilayer-stacked system-in-pacakage for software-defined-radio. *IEICE Transactions on Electronics*, E84-C(12):1730–1734, December 2001.

[17] K. Takashi et al. Ultra-high-density interconnection technology of three-dimensional packaging. *Microelectronics Reliability*, 43:1267–1279, 2003.

[18] M.S. Bakir et al. Sea of Leads (SoL) Ultrahigh Density Wafer-Level Chip Input/Output Interconnections for Gigascale Integration (GSI). *IEEE Transactions On Electron Devices*, 50(10):2039–2048, October 2003.

[19] E. Beyne. Multilayer thin-film technology enabling technology for solving high-density interconnect and assembly problems. *Nuclear Instruments and Methods in Physics Research Section A*, 509(1-3):191–199, 2003.

[20] C. Schwarz et al. Measurements with Si and GaAs pixel detectors bonded to photon counting readout chips. *Nuclear Instruments and Methods in Physics Research Section A*, 466(1):87–94, 2001.

[21] M. Chmeissani et al. Charge Sharing Measurements of pixilated CdTe using Medipix-II chip. In *Proceedings of the 21st IEEE Instrumentation and Measurement Techniques Conference, Como, Italy, 18-20 May 2004*, pages 787–791.

[22] A. G. Holmes-Siedle and L. Adams *Handbook of radiation effects.* Oxford University Press, 2002.

[23] W. J. Snoeys et al. A New NMOS Layout Structure for Radiation Tolerance. In *Proceedings of the IEEE Nuclear Science Symposium and Medical Imaging Conference, San Diego, USA, November 2001*, 2001.

[24] A. Giraldo. *Evaluation of deep-submicron technologies with radiation tolerant layout for electronics in the LHC environments*. PhD thesis, University of Padova, December 1998. Available at: http://wwwcdf.pd.infn.it/cdf/sirad/giraldo/tesigiraldo.html.

[25] R.C. Lacoe Improving Integrated Circuit Performance Through the Application of Hardness-by-Design Methodology. *IEEE Transactions on Nuclear Science*, 55(4):1903–1925, August 2008.

[26] D. San Segundo Bello et al. An interface board for the control and data acquisition of the Medipix2 chip. *Nuclear Instruments and Methods in Physics Research Section A*, 509(1-3):164–170, 2003.

[27] M. Campbell et al. Readout for a 64 x 64 pixel matrix with 15-bit single photon counting. *IEEE Transactions on Nuclear Science*, 45(3):751–753, 1998.

[28] C.Posch et al. A Dual-Line Optical-Transient Sensor with On-Chip Precision Time-Stamp Generation. In *Proceedings of the IEEE International Solid-State Circuits Conference, San Francisco, USA, February 2007*, 2007.

[29] P. Seller et al. Two Approaches to hybrid X-ray pixel array readout. *Proceedings of the SPIE*, 3774:30–37, 1999.

[30] C. Kapnistis et al. An Asynchronous Pixel Architecture for Simultaneous Radiation Imaging and Spectroscopy on a Real-Time Basis. *IEEE Transactions on Nuclear Science*, 49(4):1802–1807, August 2002.

[31] B. Pain and E.R. Fossum. Approaches and analysis for on-focal-plane analog-to-digital conversion. *Proceedings of the SPIE*, 2226:1–11, 1994.

[32] S.K. Mendis et al. Design of a low-light-level image sensor with on-chip sigma-delta ADC. *Proceedings of the SPIE*, 1900:31–39, 1993.

[33] U. Ringh et al. Readout concept employing a novel on chip 16 bit ADC for smart IR focal plane arrays. *Proceedings of the SPIE*, 2745:99–110, 1996.

[34] Z. Zhou et al. MOS active pixel sensor with on chip successive approximation ADC. *IEEE Transactions on electron devices*, 44(10):1759–1763, October 1997.

[35] S. Decker et al. A 256x256 CMOS Imaging Array with Wide Dynamic Range Pixels and Column-Parallel Digital Output. In *ISSCC digest of technical papers*, pages 176–177, 1998.

[36] A. Simoni et al. 256 x 256-pixel CMOS digital camera for computer vision with 32 algorithmic ADCs on board. *Proceedings of the IEE: Circuits, Devices and Systems*, 146(4):184–190, August 1999.

[37] W. Mandl et al. MOSAD IR focal plane per pixel A/D development. *Proceedings of the SPIE*, 2745:90–98, 1993.

[38] D. Fowler. *CMOS area image sensors with pixel level A/D conversion*. PhD thesis, Stanford university, October 1995.

[39] B. Fowler et al. Techniques for pixel level analog to digital conversion. *Proceedings of the SPIE*, 3360:2–12, 1998.

[40] D. Xiao Dong Yang. *Digital pixel CMOS image sensors*. PhD thesis, Stanford university, August 1999.

[41] L. G. McIlrath. A Low-Power Low-Noise Ultrawide-Dynamic-Range CMOS Imager with Pixel-Parallel A/D Conversion. *IEEE Journal of Solid-State Circuits*, 36(5):846–853, May 2001.

[42] A. Bermak. CMOS imager with pixel level ADC: A CMOS Imager With PFM/PWM Based Analog-To-Digital Converter. In *Proceedings of the 2002 IEEE International Symposium on Circuits and Systems (ISCAS), Scottsdale, Arizona, 26-29 May 2002*, pages 53–56.

[43] J.G. Rocha et al. CMOS X-ray image sensor with pixel level A/D conversion. In *Proceedings of the 2003 European Solid States Circuits Conference (ESSCIRC), Estoril, Portugal, 16-18 September 2003*.

[44] A. Mekkaoui and J. Hoff. 30Mrad(SiO_2) radiation tolerant pixel front end for the BTEV experiment. *Nuclear Instruments and Methods in Physics Research Section A*, 465(1):166–175, 2001.

[45] L. Blanquart. FEI-2: A Front-End Readout Chip designed in a commercial 0.25μm process for the ATLAS Pixel Detector at LHC. In *Proceedings of the IEEE Nuclear Science Symposium and Medical Imaging Conference, Portland, October 19-25, 2003*.

[46] C. Bebek et al. Time-over-threshold technique for a drift chamber readout system. In *Proceedings of the 5th International Conference on Electronics for Particle Physics International Conference on Electronics for Future Colliders , Chestnut Ridge, NY, USA , 10 - 11 May 1995*, pages 121–132.

[47] M. Barbero et al. Design and test of the CMS pixel readout chip. *Nuclear Instruments and Methods in Physics Research Section A*, 517(1-3):349–359, 2004.

[48] P. Datte et al. Status of the digital pixel array detector for protein crystallography. *Nuclear Instruments and Methods in Physics Research Section A*, 421(3):576–590, 1999.

[49] S. Borkar. Does asynchronous logic design really have a future? *EE Times*, June 2003.

[50] D. Sylvester and K. Keutzer. Impact of small geometries on microarchitectures in systems on a chip. *Proceedings of the IEEE*, 89(4):467–489, April 2001.

[51] R. Ho et al. The future of wires. *Proceedings of the IEEE*, 89(4):490–504, April 2001.

[52] J.H.R. Schrader et al. Data communication in read-out systems: how fast can we go over copper wires? *Nuclear Instruments and Methods in Physics Research Section A*, 531(1-2):221–227, 2004.

[53] J.H.R. Schrader et al. Pulse-width modulation pre-emphasis applied in a wireline transmitter, achieving 33 dB loss compensation at 5-Gb/s in 0.13-/spl mu/m CMOS. *IEEE Journal of Solid-State Circuits*, 41(4):990–999, 2006.

Chapter 5

Pixel front-end electronics

Figure 5.1 shows a block diagram of the pixel front-end electronics.

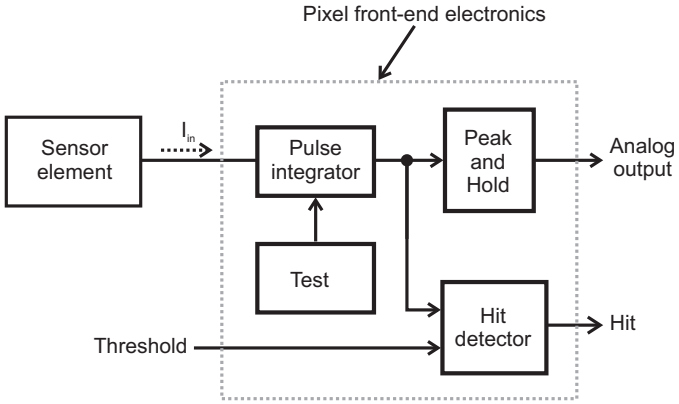

Figure 5.1: Block diagram of the pixel front-end electronics.

The current generated by the photon interaction in the sensor is the input to the *pulse integrator* described in section 5.1. The output of the integrator is a measure of the collected charge which will be used as the input to the hit detection and peak and hold circuits. In the *hit detector* described in section 5.2, the output of the integrator is compared to a threshold to detect if the signal is above the intrinsic system noise. If this is the case, the peak value of the integrator's output is held by the *peak-and-hold* circuit described in section 5.3. The outputs of the hit detector (*Hit* in the figure) and the peak-and-hold (*Analog output* in the figure) will be the inputs to the analog-to-digital converter (ADC) described in chapter 6. Finally, section 5.4 shows the layout of the front-end electronics included in one of the prototype chips.

5.1 Pulse integrator

Chapter 3 has shown how the charge generated in a semiconductor-based detector by a photon interaction induces a current pulse in the collecting electrodes of the sensor. This pulse has a shape, rise-time and amplitude that are functions of the geometry and the electric field distribution within the sensor. Although the height of this pulse is somewhat proportional to the energy of the incident particle, this proportionality depends on many parameters, including operating conditions, sensor type, etc. Integrating this current pulse, however, gives a good measure of the collected charge, which in turn is proportional to the energy deposited by the photon in the detector.

In order to be independent from the characteristics of the sensor, and in particular of its intrinsic capacitance, the integrator should present an impedance to the detector as close to zero as possible so as to collect all the charge generated in the interaction. This can be achieved by using a *transimpedance amplifier* such as the one shown in Figure 5.2.

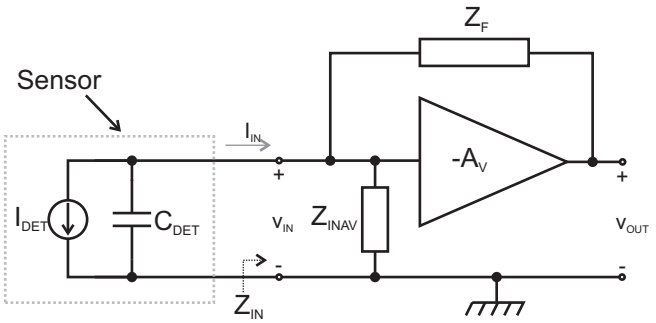

Figure 5.2: Basic transimpedance amplifier topology. Z_{INAV} represents the input impedance of the voltage amplifier, which includes the input capacitance and resistance.

The equivalent input impedance (Z_{IN}) of this circuit can be calculated as:

$$Z_{IN}(s) = \frac{V_{IN}(s)}{I_{IN}(s)} = \frac{Z_F(s) \cdot Z_{INAV}(s)}{Z_F(s) + [(1 + A_V) \cdot Z_{INAV}(s)]} \tag{5.1}$$

If the input impedance of the amplifier $Z_{INAV}(s)$ is made much larger than $Z_F(s)$, and for a relatively large value of the gain A_V, the input impedance simplifies to:

$$Z_{IN}(s) = \frac{V_{IN}(s)}{I_{IN}(s)} = \frac{Z_F(s)}{1 + A_V} \tag{5.2}$$

If the feedback impedance is resistive ($Z_F(s) = R_F$), the circuit is a *transresistance amplifier**. The sensor current is directly converted to a voltage at the output of the amplifier. This voltage still needs to be integrated to obtain a measure of the collected charge. Transresistance amplifiers are rarely used in

*It is very common in the literature to find *transresistance* amplifiers referred to as *transimpedance* amplifiers.

radiation detection except for very high particle rates [1], due to its somewhat complicated design.

If the feedback impedance is capacitive ($Z_F(s) = 1/(s \cdot C_F)$), the circuit is referred to as a *charge sensitive amplifier* (CSA for short). In this case the current from the sensor is integrated into the feedback capacitance and thus the output voltage of the amplifier is proportional to the collected charge.

The equivalent input capacitance of a CSA is:

$$C_{IN} = C_F \cdot (1 + A_V) \tag{5.3}$$

This capacitance can be made larger than the detector capacitance C_{DET} for moderate to large values of A_V.

The charge-to-voltage transfer function is then:

$$A_Q(s) = \frac{V_{OUT}(s)}{Q_{IN}(s)} = -\frac{A_V}{1 + A_V} \cdot \frac{1}{C_F} \tag{5.4}$$

which, for large values of A_V can be approximated to $-1/C_F$. The value of C_F must be kept small in order to have a large gain A_Q. If C_F is too small, however, the output of the amplifier can saturate at relatively small input charges.

The feedback capacitor C_F has to be discharged after each interaction so that the output voltage of the amplifier returns to its DC operating point and a new interaction can be processed. The discharge of the feedback capacitor can be made either periodically using pulsed reset techniques, or continuously (e.g. with a feedback resistor). The first approach is limited to synchronous applications when the events are expected at precisely predictable time slots, whereas the second is more general.

Continuous discharge with a feedback resistor has two major drawbacks. First, the use of a purely resistive feedback would produce high DC level shifts at the output due to the leakage current from the detector. And secondly, the value of the resistor has to be large in order to allow full collection of the charge from the sensor before the discharge of the capacitor begins, but it is difficult to realize integrated resistors of large value, specially in pixel detectors where the size of the processing electronics must be kept as small as possible. As a consequence, more elaborate methods to discharge the feedback capacitor and compensate for the detector leakage current are used, such as constant current feedback or active feedback techniques [2, 3].

5.1.1 Specifications

The most important specifications for the design of the pulse integrator are the *input noise*, the *gain* and the maximum allowed *detector leakage current*.

The noise specification of a detector readout system is typically given as the *equivalent noise charge* (ENC), which is defined as the ratio of the total integrated noise at its output to the signal amplitude due to one electron*.

The total equivalent noise charge (ENC) can be calculated as:

*An equivalent definition for the ENC is the amount of charge that, if applied suddenly to the input terminals of the system, would give raise to an output voltage equal to the RMS level of the output due only to noise.

$$ENC^2 = ENC_d^2 + ENC_f^2 + ENC_0^2 \tag{5.5}$$

where ENC_d is the ENC due to the thermal noise and ENC_f is the ENC due to 1/f noise, both of the input transistor, and ENC_0 is the ENC due to the the detector leakage current and the associated circuitry.

The ENC due to the channel thermal noise of the input transistor (ENC_d) is a function of the total input capacitance ($C_t = C_d + C_p + C_f$), the transconductance g_m of the transistor and the shaping time τ_s:

$$ENC_d^2 \propto \frac{C_t^2}{g_m \tau_s} \tag{5.6}$$

where C_d is the detector capacitance, C_p the parasitic capacitance at the input and g_m is the transconductance of the input CMOS transistor. To reduce this noise, low total input capacitance, high power consumption (proportional to g_m) and long shaping times can be used.

The ENC due to 1/f noise (ENC_f) in CMOS transistors is proportional to the total input capacitance C_t and inversely proportional to the area of the device:

$$ENC_f \propto \frac{C_t^2}{W \cdot L} \tag{5.7}$$

The ENC due to the detector leakage current and the associated circuit (ENC_0) is:

$$ENC_0^2 \propto I_0 \tau_s \tag{5.8}$$

where I_0 represents the sum of the effects of the detector leakage current and the bias circuit. As opposed to ENC_d, in order to reduce the noise due to the detector leakage current, short shaping times should be used.

When designing the readout circuitry for a given detector, a trade-off between ENC, speed (τ_s) and power consumption (g_m) has to be performed to meet the required properties of the detection system.

The *gain* is derived from the the maximum charge to be detected, and is directly related to the supply voltage. Assuming an output voltage swing between V_{DD}-300 mV and V_{SS}+300 mV and that for high energy photons the detector will be made of GaAs or Cd(Zn)Te, the gain G is found as:

$$G = \frac{V_{MAX} - V_{MIN}}{E_{phMAX}} \cdot \epsilon_{MAX} = \frac{V_{DD} - 0.6}{100keV} \cdot 4.4eV = 52.8\mu V/electron \tag{5.9}$$

where a voltage of 1.8V is taken for V_{DD} and the maximum ionization energy used (ϵ_{MAX}) is that of Cd(Zn)Te (4.4 eV).

The *detector leakage* refers to the maximum DC leakage current from the detector that needs to be compensated for in the integrator. For this design, the same specification as for the Medipix2 chip was used [4].

The basic specifications for the integrator are summarized in Table 5.1.

Table 5.1: Specifications for the integrator.

Name	Value	Unit
ENC	200	electrons
Gain	52.8	μV/electron
Maximum detector leakage current (electron collection)	-330 to 0	μA/cm^2
Maximum detector leakage current (hole collection)	0 to 660	μA/cm^2

5.1.2 Design of the integrator

The integrator has been implemented as a charge sensitive amplifier with active feedback [2, 4]. Figure 5.3 shows the full transistor implementation of this circuit. This circuit is sensitive for both positive and negative charge collection.

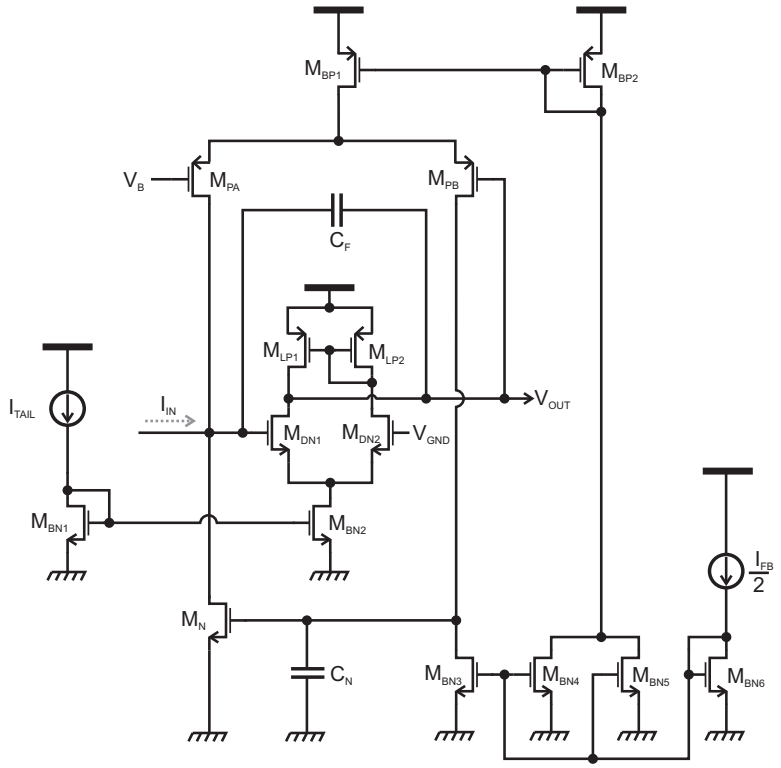

Figure 5.3: Implementation of the integrator showing all the necessary transistors. The bias network is formed by transistors M_{BP1}, M_{BP2}, M_{BN1}, M_{BN2}, M_{BN3}, M_{BN4}, M_{BN5} and M_{BN6}.

Transistors M_{DN1}, M_{DN2}, M_{LP1} and M_{LP1} form a differential amplifier which is biased by I_{TAIL}, M_{BN1} and M_{BN2}. C_F is the feedback capacitance. The active feedback network used to discharge the capacitor and compensate

for the leakage current from the sensor consists of a differential pair of pMOS transistors (M_{PA} and M_{PB}), an nMOS transistor (M_N) working as a current source controlled by the voltage across C_N and two current sources formed by transistors M_{BP1} and M_{BN3}. No output stage is needed for this differential amplifier since its load will only be the input capacitances of the peak-and-hold and hit-detection blocks.

The *active feedback* discharges the feedback capacitance and compensates for the leakage current from the sensor. The transistors in the feedback network (M_{PA}, M_{PB} and M_N), as well as C_N and C_{FB} are designed so that the following identity holds:

$$\frac{C_N}{g_{mN}} > \frac{C_F}{g_{mP}} \gg t_c \tag{5.10}$$

where g_{mN} is the small-signal transconductance of transistor M_N, g_{mP} is the small-signal transconductance of transistors M_{PB} and M_{PA} and t_c is the duration of the input current pulse, which is approximately equal to the collection time of the detector.

The noise from the OTA (transistors M_{DN1}, M_{DN2}, M_{LP1} and M_{LP1} and M_{BN2}) is the dominant noise source and it can be calculated as:

$$V_{neq}^2(f) = \left(\frac{16}{3}\right) kT \left(\frac{1}{g_{mDN1}}\right) (1 + g_{mLP2}) \tag{5.11}$$

which leads to the well known design constraint of large g_{mDN1} in order to minimize the thermal noise contribution.

Table 5.2 shows the final sizes of the transistors in the circuit shown in Figure 5.3.

Table 5.2: Sizes of the transistors in the circuit shown in Figure 5.3

Transistor name	Width (μm)	Length (μm)
M_{BN1}, M_{BN2}	1.5	8
M_{BN3}, M_{BN4}, M_{BN5}, M_{BN6}	0.5	5
M_{BP1}, M_{BP2}	1	5
M_{PA}, M_{PB}	2	5
M_{LP1}, M_{LP2}	1.5	4
M_{DN1}, M_{DN2}	10	0.5
M_N	0.42	10

Table 5.3 shows the feedback capacitance and bias values.

Table 5.3: Sizes of the transistors in the circuit shown in Figure 5.3

Name	Value	Units
C_F	8	fF
C_N	345	fF
V_{DD}	1.8	V
V_B	900	mV
V_{GND}	900	mV
$I_{FB/2}$	4	nA
I_{TAIL}	800	nA

The capacitor C_N is implemented as a MOS capacitor and the feedback capacitor is implemented as a poly-nwell capacitor.

Figure 5.4 shows an example simulation of the output voltage of the integrator.

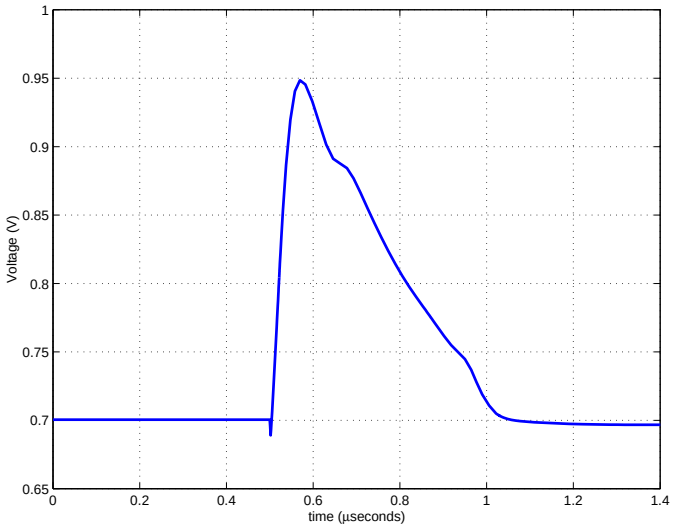

Figure 5.4: Example simulation of the output voltage of the integrator.

5.2 Hit detector

The purpose of the *hit detector* is to decide if the signal at the output of the integrator is the result of a photon interaction or is caused by the intrinsic noise of the system. In the first case, the hit detector will indicate to the analog-to-digital converter that it can start a conversion.

Figure 5.5 shows a block diagram of the hit detector.

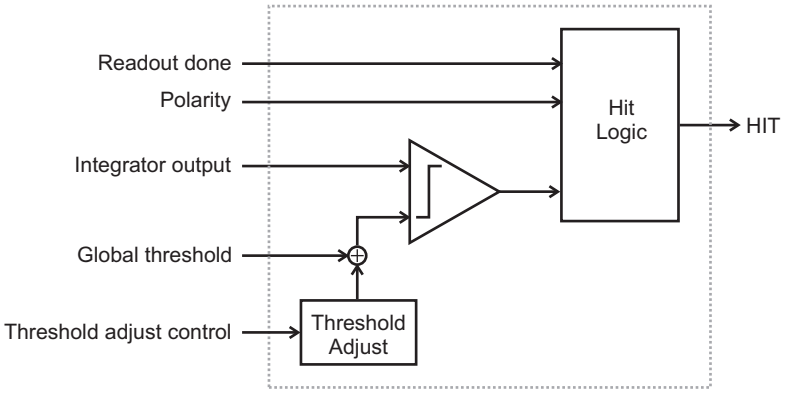

Figure 5.5: Block diagram of the hit detector.

The output voltage of the integrator and a threshold reference are the inputs to a comparator. The threshold reference is generated from a global threshold and a local (at pixel level) threshold adjustment. The output of the comparator is the input to the digital hit logic which ultimately generates the output *hit* signal.

The global threshold is typically generated outside of the pixel array by a DAC (e.g. in the periphery of the chip) and then distributed to all the pixels in the array. The local threshold adjustment is applied using a mechanism such as the one found in the Medipix2 chip [4]. It can be performed for example by a low-resolution DAC which adds/substracts a value to the global threshold value. This DAC can be set individually in each pixel by programming the adequate value into the *pixel configuration* block shown in Figure 4.3.

The logic after the comparator has two functions. First, it takes into account the polarity of the signal from the detector in order to detect positive or negative pulses from the integrator. And second it makes sure that the output of the comparator is propagated to the ADC only when the previous result of a photon hit has been read from the pixel.

The following subsections describe the design of the comparator and the hit logic in more detail.

5.2.1 Design of the comparator

Figure 5.6 shows a block diagram of the comparator.

The output voltage of the integrator is converted to a current using a transconductor (g_m in the figure). The global and local threshold adjustments are generated using current-steering DACs and are added to the output of the transconductor. The sum of the output of the transconductor and the threshold adjustments is the input to a current-mode comparator.

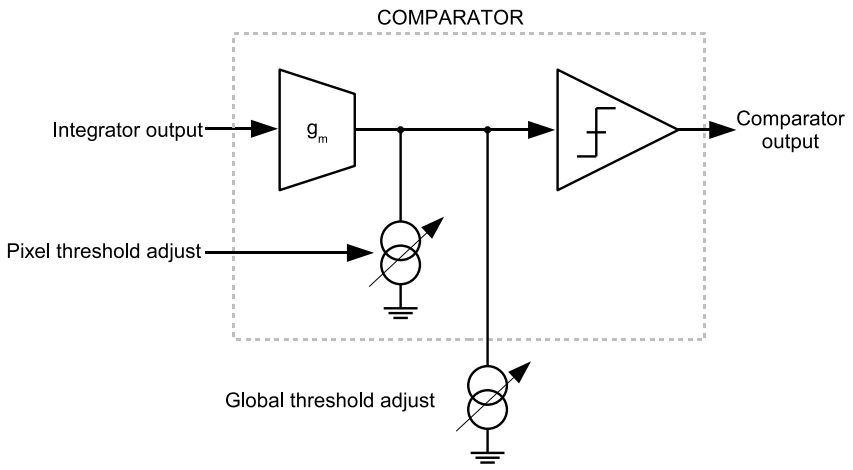

Figure 5.6: Block diagram of the comparator.

The current-mode comparator[5] is shown in Figure 5.7.

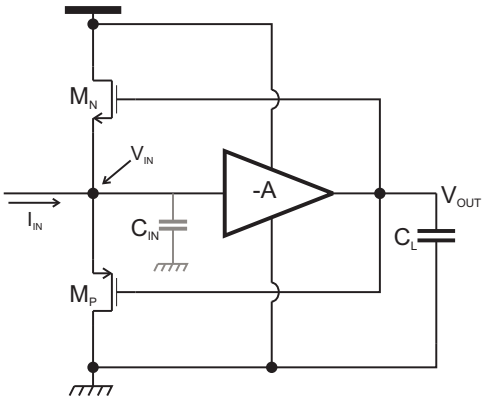

Figure 5.7: Schematic drawing of the comparator.

The comparator consists of an inverting voltage amplifier and the two feedback transistors M_N and M_P. The intrinsic input capacitance of the comparator (C_{IN}) is composed of the input capacitance of the amplifier and the source capacitances of M_N and M_P. The load capacitance C_L consists of the input capacitance of the hit logic.

It is clear from Figure 5.7 that the gate-source voltages (V_{GS}) of transistors M_N and M_P are equal. M_N will conduct for positive V_{GS} values and M_P will conduct for negative V_{GS} values:

$$V_{GS} = V_{GSN} = V_{GSP} = V_{OUT} - V_{IN} \tag{5.12}$$

It is also evident that both transistors are always operating in saturation, as their drain-source voltage will always be larger than their overdrive voltage

($|V_{DS}| > |V_{GS} - V_T|$).

The input current of the comparator can be calculated as:

$$I_{IN} = I_{int} - (I_{THRg} + I_{THRa}) \tag{5.13}$$

where I_{int} is the output current of the transconductor shown in Figure 5.6, which is proportional to the output of the integrator, I_{THRg} is the global threshold and I_{THRa} is the local threshold adjust.

If this current is equal to zero, both M_N and M_P are turned off or conduct current depending on the value of the supply voltage and the threshold voltages of the transistors. If $V_{DD} < |V_{THN}| + |V_{THP}|$ the two transistors are turned off (or conduct a very small current). If $V_{DD} > |V_{THN}| + |V_{THP}|$ both transistors would be conducting current between the positive supply and ground, and this current will be fixed by the values of V_{IN} and V_{OUT}.

If a positive current begins to flow into the circuit it cannot flow through M_P either because this transistor is turned off or because the current flowing through M_P is fixed by V_{OUT} and V_{IN}. The input current will thus begin to charge C_{IN}, increasing the voltage across the capacitor (V_{IN}) which results in V_{OUT} becoming more negative. The net result is that V_{GS} in Equation 5.12 becomes negative, causing M_P to conduct (more) current while M_N is driven (deeper) into the cut-off region. As M_P conducts more current, the input current is split between the current charging the input capacitance and the current flowing through M_P until the value of $V_{OUT} - V_{IN}$ is such that all the input current flows through M_P. For a negative input current the behavior of the circuit is similar, but now the input current ends flowing through transistor M_N.

Summarizing the previous paragraph: if I_{IN} is positive the output voltage will be close to the negative power supply voltage (ground in the drawing) and if the current is negative the output voltage will be close to the positive power supply voltage. A CMOS inverter can be added to the output of the comparator to obtain a logic level that can be used in the hit detector logic.

From a power consumption point of view the current drawn from the power supply by the transistors M_N and M_P should be zero when $I_{IN} = 0$. On the other hand, if there is some current flowing from the supply across the transistors when $I_{IN} = 0$ (i.e. the transistors are not completely turned off), the comparator will be able to switch faster. Simulations showed that the comparator switched fast enough when the feedback transistors were turned off for $I_{IN} = 0$. This means that a very low value of supply voltage can be used (1 V in our case) and that the amplifier can be implemented as a minimum-sized CMOS inverter. This, in turn leads to a small area occupied by the comparator compared to the area of the input amplifier or the peak-and-hold circuit. As a result of choosing a supply voltage of 1 V for the comparator, it was decided to use this supply voltage for all the digital circuitry in the pixel, including the digital portion of the analog-to-digital converter explained in chapter 6 and the pixel readout block explained in chapter 7.

The implementation of the comparator is shown in Figure 5.8.

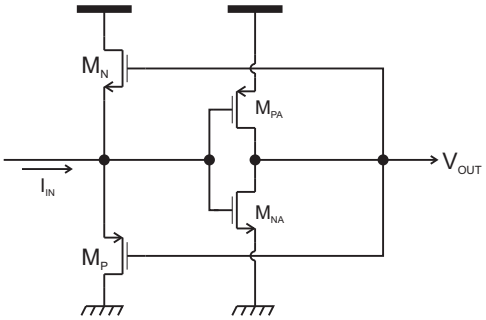

Figure 5.8: Transistor implementation of the current comparator.

The sizes of all transistors have to be small in order to have a small C_{IN}, and the W/L ratio of the transistors in the inverter has to be high for a large amplification. A very important feature of this comparator is that there are no matching requirements for the transistors M_N and M_P, which means that they can be made quite small. The final sizes are listed in Table 5.4.

Table 5.4: Sizes of the transistors in the circuit shown in Figure 5.8

Transistor name	Width (μm)	Length μm)
M_N	0.4	0.24
M_P	1	0.24
M_{PA}	1	0.24
M_{NA}	0.4	0.24

5.2.2 Design of the digital hit logic

The digital hit detector logic is shown in the Figure 5.9.

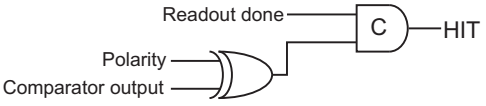

Figure 5.9: The hit detector logic.

The output of this block (*hit*) must go high when a hit is detected by the comparator and at the same time the readout circuitry is inactive, i.e. no data is being read from the pixel (i.e. *readout_done* is high). *Hit* goes low only when no photon interaction is detected and at the same time the readout circuit is active (*readout_done* is low). If there are more photon hits detected before the result of the first photon hit has been read from the pixel, there must be no changes in *hit*.

Because the pixel circuitry is sensitive to both positive and negative charges, the output of the comparator will depend on the polarity of the input signal. This is handled by the XOR gate shown in the figure.

The output of the comparator is used as one of the inputs to a so-called *C*

*element**. The other input to the C element is one of the outputs of the pixel readout block explained in section 7.1.1, which indicates that the ADC is empty and the readout block is inactive.

5.3 Peak and hold

The output of the integrator described in section 5.1 is a voltage pulse with a fast rise time in the order of a few nanoseconds (determined by the gain of the amplifier and the load capacitance) and a somewhat slower fall time (determined by the feedback network but typically of about a few hundreds of nanoseconds). The information that needs to be processed by the analog-to-digital converter is in the peak of this pulse, and not in its shape. The peak-and-hold circuit holds this peak value constant during the conversion by the ADC.

If a conventional sample-and-hold circuit were used for this purpose, it would need a very accurate time resolution in order to sample exactly the peak value. Furthermore, there should be one such circuit located in every pixel of the imaging array, and each one should work independently from all the others. A much simpler way to capture the peak value of the amplifier output is to use a *peak-and-hold* circuit [6, 7, 8, 9, 10]. Figure 5.10 shows a circuit that realizes such a function.

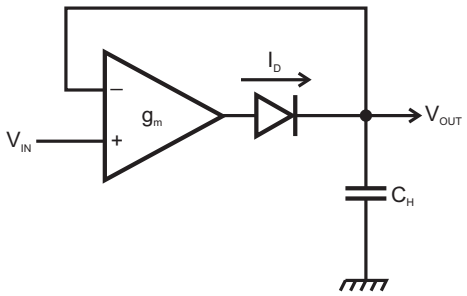

Figure 5.10: Basic peak and hold circuit.

The circuit consists of a differential transconductor (g_m), a diode and a hold capacitor (C_H). While $V_{IN} > V_{OUT}$ the output current from the transconductor is equal to:

$$I_D(t) = g_m \cdot (V_{IN}(t) - V_{OUT}(t)) \tag{5.14}$$

This current is integrated in the hold capacitor, producing an output voltage V_{OUT} equal to:

$$V_{OUT}(t) = \frac{1}{C_H} \int I_D(t)dt \tag{5.15}$$

At the moment that V_{OUT} becomes equal to V_{IN} the direction of I_D would have to change, discharging the capacitor. But the diode prevents this from

*The operation of the *C element* is described in more detail in section C.2.1. Briefly, its output will only change when both its inputs have changed and are equal. In all other cases its output is kept at the last defined output (i.e. when both inputs were equal).

happening, and the capacitor has no discharge path. As a result, V_{OUT} keeps the peak value of V_{IN}.

5.3.1 Design of the peak and hold

The circuit can be implemented in a conventional CMOS technology as shown in Figure 5.11.

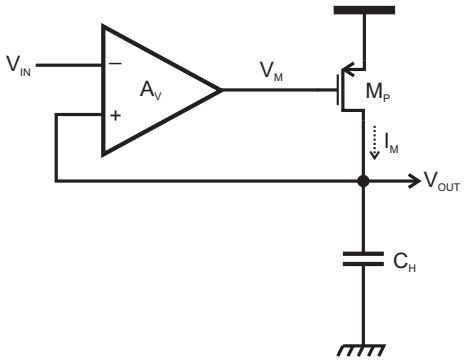

Figure 5.11: A simple CMOS implementation of a peak and hold circuit.

The transconductor in Figure 5.10 is implemented in Figure 5.11 by the differential amplifier and the pMOS transistor. The diode characteristic is obtained by the $I_D(V_{GS})$ characteristic of the pMOS transistor. The voltage at the gate of the transistor controls the value of I_M, and it is equal to:

$$V_M(t) = A_V \cdot (V_{OUT}(t) - V_{IN}(t)) \tag{5.16}$$

The voltage across the capacitor is

$$V_{OUT}(t) = \frac{1}{C_H} \int I_M(t)dt \tag{5.17}$$

If the input voltage V_{IN} is higher than the voltage across the capacitor V_{OUT}, the difference voltage at the input of the amplifier $(V_{OUT} - V_{IN})$ will generate a negative transition in V_M, which will force the transistor to start conducting current. This current (I_M) will charge the capacitor C_H until V_{OUT} is equal to V_{IN}, at which point the transistor will be turned off. As a result V_{OUT} will track V_{IN} until the input voltage reaches its peak value and begins to decrease. If there is no discharge path for the capacitor, it will hold the peak value of V_{IN}.

The loop will control I_M so that:

$$I_M(t) = C_H \cdot \frac{\partial V_{IN}(t)}{\partial t} \tag{5.18}$$

This simple implementation of the peak-and-hold circuit has nevertheless several limitations. For example, charge coupling through the gate-drain capacitance of the transistor, variations in the drain capacitance of the transistor, finite gain and common mode rejection ratio of the amplifier, offset voltage at

the input of the amplifier, etc. A more detailed analysis of these issues can be found in [8, 9].

Figure 5.12 shows the full transistor implementation of the peak-and-hold circuit used in the pixADC4 prototype chip.

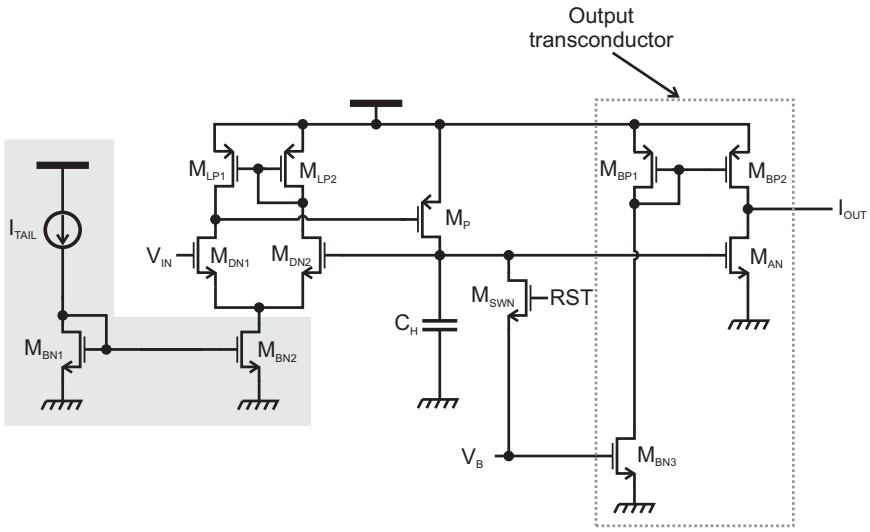

Figure 5.12: Implementation of the peak and hold circuit. The bias circuitry is shaded in grey.

The differential amplifier in Figure 5.11 is implemented by transistors M_{DN1}, M_{DN2}, M_{LP1} and M_{LP2}. This amplifier is biased by I_{TAIL} via transistors M_{BN1} and M_{BN2}. When the ADC has finished the conversion, the hold capacitor is reset using transistor M_{SWN} as a switch. The control signal RST is the result of a logic OR between the main *reset* and the signal generated in the ADC to indicate that the conversion is finished.

A transconductor is added to the circuit to convert the voltage held at the capacitor to a current, as the ADCs explained in chapter 6 need a current input.

Because the DC value at the input of the amplifier will be equal to V_B (see Figure 5.3),the voltage at the capacitor will also have to be equal to V_B after a reset. Transistor M_{SWN} resets the peak and hold by charging the hold capacitor to V_B. Transistors M_{BN3}, M_{BP3} and M_{BP2} are used to bias the transconductor. Transistor M_{BN3} has the same dimensions as M_{AN}, and its gate-source voltage is equal to V_B. The resulting current is used to bias M_{AN} to make sure that the output current is zero when the capacitor voltage is reset to the input DC value of V_B.

The hold capacitor was implemented as a metal-insulator-metal (MiM) capacitor. The value needed was 2.2 pF.

Table 5.5 shows the sizes of the transistors in the circuit shown in Figure 5.12.

Table 5.5: Sizes of the transistors in the circuit shown in Figure 5.12

Transistor name	Width (μm)	Length (μm)
M_{BN1},M_{BN2}	1	8
M_{DN1},M_{DN2}	10	0.5
M_{LP1},M_{LP2}	1	4
M_{SOP}	0.8	10.92
M_{SWN}	4	0.24
M_{BP1},M_{BP2}	0.8	3
M_{AN},M_{BN3}	0.8	8

Figure 5.13 shows some waveforms from a simulation of the complete front-end circuitry.

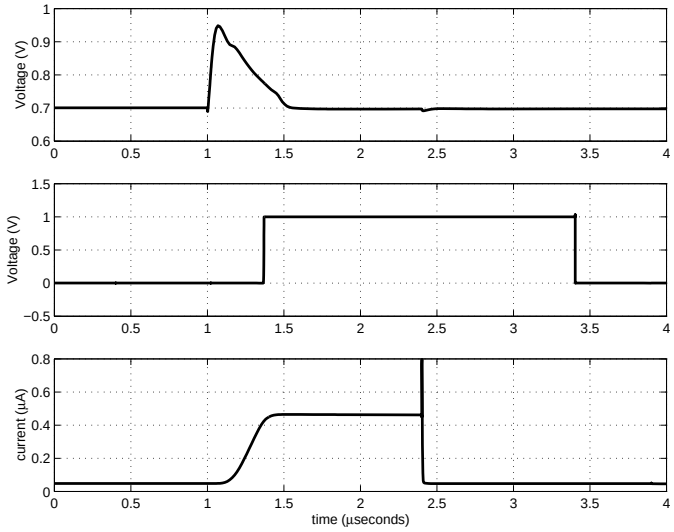

Figure 5.13: Results of a simulation of the complete front-end. From top to bottom: output of the integrator, output of the hit detector, and output of the peak and hold.

The top waveform shows the output of the integrator. The waveform in the middle shows the output of the hit detector and the waveform at the bottom shows the output of the peak and hold circuit.

Once the conversion is finished, the peak and hold circuit is reset. The output of the hit detector, however stays high until the data has been readout from the pixel, as explained in Section 5.2.2.

5.4 Layout of the front-end electronics

Figure 5.14 shows the layout of the front-end electronics as found in the pix-ADC4 prototype chip.

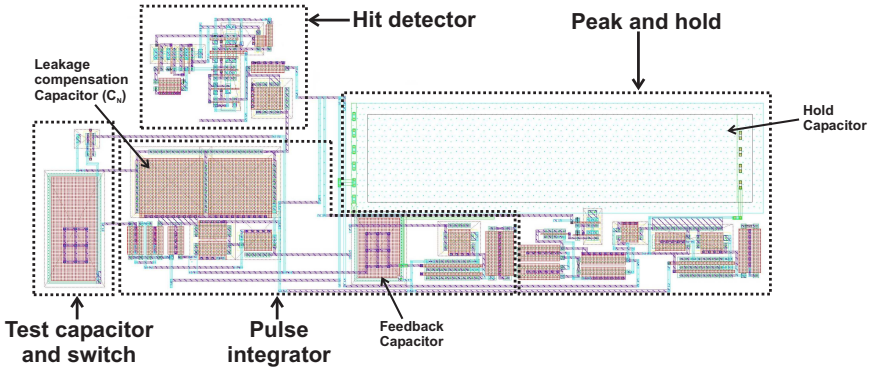

Figure 5.14: Layout of the pixel front-end electronics in the pixADC4 prototype chip. The dimensions of the circuit in the figure are 50 μm by 130 μm.

The large structure in the peak-and-hold block is the hold capacitor C_H. In the input amplifier, the capacitor C_N was implemented as a MOS gate capacitance, and it is made out of two such capacitances in parallel due to limitations in maximum poly-silicon area. These capacitors can be seen right below the *hit detector*. As explained earlier in this chapter, the integrating capacitor was implemented as a poly-nwell capacitor. The block labeled *Test capacitor and switch* correspond to the circuitry explained later in B.3.

5.5 Summary and conclusions

The charge generated in the sensor as a result of a photon interaction induces a current in the collecting electrodes that is the input to the pixel processing electronics chip. To obtain the value of this charge, the current entering the processing electronics has to be integrated. The simplest way to integrate this current is to use a *charge sensitive amplifier*. An additional feedback network is needed to reset the feedback capacitor of the charge sensitive amplifier and to compensate for the leakage current from the sensor.

The output of the integrator is used as the input to both a *hit detector* and a *peak-and-hold circuit*. The hit detector is used to ascertain that the signal was caused by a photon interaction and is not due to the intrinsic system noise. The output of the hit detector will indicate to the pixel ADC that it can start the conversion of the signal at the output of the peak-and-hold circuit. The peak-and-hold circuit is used to hold the peak value of the input amplifier, which is the input to the ADC described in the next chapter.

Bibliography

[1] F. Anghinolfi et al. A transimpedance amplifier using a novel current mode feedback loop. In *Proceedings of the 7th European Symposium on Semiconductor Detectors, New Developments in Radiation Detectors , Schloss Elmau, Germany , 7 - 10 May 1995*, pages 435–439.

[2] F. Krummenacher. Pixel detectors with local intelligence: an IC designer point of view. *Nuclear Instruments and Methods in Physics Research Section A*, 305(3):527–532, 1991.

[3] G. De Geronimo et al. Front-end electronics for imaging detectors. *Nuclear Instruments and Methods in Physics Research Section A*, 471(1-2):192–199, 2001.

[4] X. Llopart et al. Medipix2, a 64k pixel read out chip with 55 μm square elements working in single photon counting mode. *IEEE Transactions on Nuclear Science*, 49(5):2279–2283, October 2002.

[5] H. Träff. Novel approach to high speed CMOS current comparators. *Electronics Letters*, 28(3):310–312, January 1992.

[6] M.W. Kruiskamp and D.M.W. Leenaerts. A CMOS peak detect sample and hold circuit. *IEEE Transactions on Nuclear Science*, 41(1):295–298, February 1994.

[7] K. Koli and K. Halonen. Low voltage MOS-transistor-only precision current peak detector with signal independent discharge time constant. In *Proceedings of the 1997 IEEE International Symposium on Circuit and Systems*, pages 1992–1995.

[8] G. de Geronimo et al. Analog CMOS Peak Detect and Hold Circuits. Part 1. Analysis of the Classical Configuration. *Nuclear Instruments and Methods in Physics Research Section A*, 484(1-3):533–543, 2002.

[9] G. de Geronimo et al. Analog CMOS peak detect and hold circuits Part 2. The two phase offset-free and derandomizing configuration. *Nuclear Instruments and Methods in Physics Research Section A*, 484(1-3):544–556, 2002.

[10] P. O'Connor et al. Amplitude and time measurement ASIC with analog derandomization. *Nuclear Instruments and Methods in Physics Research Section A*, 505(1-2):352–357, 2003.

Chapter 6

Pixel-level ADCs

The circuits described in the previous chapter process the signal from the sensor and generate the two signals that are used by the ADC described in this chapter. The output of the *peak-and-hold* described in section 5.3 is the analog signal that must be converted by the ADC and the output of the *hit detector* described in section 5.2 is the digital signal that indicates that the conversion can take place.

Section 6.1 lists the basic specifications of the pixel level ADCs. Next, section 6.2 lists the different existing types of analog-to-digital conversion techniques to find the best suited for our application. From these, two architectures are chosen for further investigation. The first type is the successive approximation, which is explained in detail in section 6.3. The other type is the algorithmic ADC and it is explained in section 6.4. Finally, section 6.5 offers a comparison of these two structures with respect to the system that is being designed.

6.1 ADC specifications

In this section, an attempt is made at extracting a number of specifications for the design of the ADCs. Given that the system is designed without a clear specific application in view, a number of assumptions and considerations are made.

Typically, an ADC is specified by its sample rate and number of bits, besides the area and power constraints common to all integrated circuits. The sample rate is related to the maximum bandwidth of the input signal and the number of bits is fixed by the signal-to-noise ratio and the maximum signal level that needs to be achieved for the specific application.

The sampling frequency for an ADC is usually related to the design of the sample and hold stage and to the overall speed of the converter. In our case, the peak-and-hold circuit explained earlier in section 5.3 is not considered a part of the ADC described in this chapter*. In this system the bandwidth of the input signal is equivalent to the photon rate. As explained earlier in section 4.1.1, a photon rate of 10^6 photons/second/mm^2 is assumed in this system. If a pixel

*However, in order to have a fair comparison with other ADC types, the power consumed by the peak-and-hold is added to the power consumed by the ADC when evaluating the ADC figure of merit, later in Sections 6.3.3 and 6.4.2.

area of 100 μm x 100 μm is assumed, we end up with a photon rate of 10^4 photons/second per pixel. This rate, however, is not uniform but depends on the nature of the source. To account for statistical variations in the distribution of the photons and to allow higher peaks of photon intensity, the ADC has to be designed for a higher sample rate. Additionally, as explained earlier in chapter 5, the signal processing in the front-end electronics also needs some time. After some simulations, a sample rate of 1 MSamples/s (or equivalently, a conversion time of 1μs) was taken as specification for this design.

At this point, and considering the lack of a well specified application for this system, it was decided to fix the number of bits to the relatively low value of four. This eases the design of the ADC and allows to explore the limitations in the circuits preceding and following the converter.

The power consumption requirement was also defined for the complete pixel electronics in section 4.2.1. A more specific goal for the ADC is related to the so-called figure of merit as defined in [1] and its comparison to other existing designs. This figure of merit is defined as:

$$FOM = \frac{P}{2 \cdot BW \cdot 2^N} \tag{6.1}$$

where P is the average power consumption per conversion, BW represents the frequency bandwidth of the input signal and N is the number of bits of the converter. Given the nature of the system, in our case we will use the inverse of the conversion time (i.e. f_{sample}) instead of $2 \cdot BW$. Typical values for the FOM range between 1 and 10 pJ per conversion [5]

Figure 6.1 summarizes the main specifications for the ADC.

Table 6.1: ADC specifications.

Name	Value	Unit
Sample rate	10^6	samples/second
Resolution	4	bits

6.2 Types of ADC

A first classification of analog-to-digital converters can be made between *Nyquist-rate* ADCs and *oversampling* ADCs. In a Nyquist-rate ADC the sampling frequency of the converter is approximately twice the frequency bandwidth of the input signal. In an oversampling ADC the sampling frequency is several times twice the frequency bandwidth of the input signal (the so-called *oversampling ratio*). For relatively large sample rate values and for low to medium bit resolutions, Nyquist ADCs are better suited than oversampling ADCs.

Nyquist converters can be divided into three different categories: direct conversion ADCs, logarithmic approximation ADCs and linear approximation ADCs. A *direct conversion* or "flash" ADC performs each conversion in one moment in time and for an N-bit conversion it needs 2^N parallel decisions. An N-bit *logarithmic approximation* ADC needs N different moments in time to perform the conversion, and must make one decision at each one of these moments. Finally, *linear approximation* ADCs need 2^N moments in time, and must also make one decision at each one of these moments.

Flash ADCs are very fast, but only useful for low resolutions, as the number of active elements needed for an N bits converter is approximately proportional to 2^N. Although the target resolution for this design is relatively low (4 bit), the design should be able to scale for higher resolutions in a simple manner, and thus the chosen ADC architecture should scale as linearly as possible with the resolution in terms of power and size. As a consequence, it was decided not to use a direct conversion ADC architecture. Linear approximation ADCs have a similar problem as flash ADCs in terms of scaling, as their conversion time is proportional to 2^N for N bits of resolution, and thus do not scale linearly with the resolution in terms of conversion time. Logarithmic approximation architectures offer approximately linear scaling in the number of active elements with respect to the bit resolution, and thus also in area, power and conversion time. The two most important logarithmic approximation architectures are *successive approximation* and *algorithmic*.

Based on the specifications from section 6.1, two logarithmic approximation architectures were chosen for further investigation: a successive approximation ADC and an algorithmic ADC. The successive approximation ADC is explained in section 6.3, and the algorithmic in section 6.4.

6.3 Successive approximation ADC

Figure 6.1 shows the block diagram of a successive approximation ADC. It consists of a comparator, a digital-to-analog converter (DAC) and a digital control block.

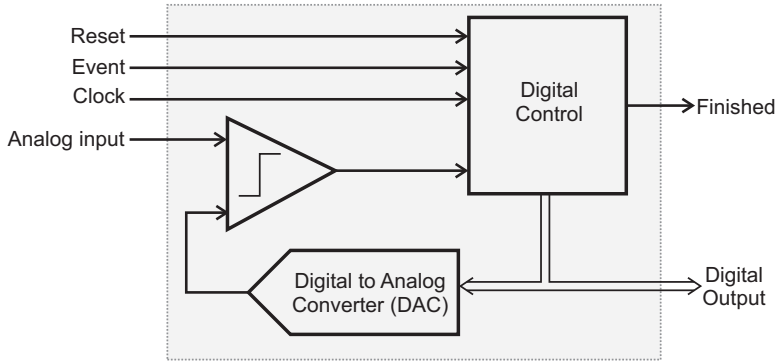

Figure 6.1: Block diagram of a successive approximation ADC.

Analog input is the output current of the peak-and-hold circuit described in section 5.3 and the signal that has to be converted to a digital value. *Event* corresponds to the output of the hit detector block from section 5.2 and is used to notify the ADC that it can start a conversion. *Reset* is used to set the contents of the ADC to a known value before starting a conversion. The *clock* signal is used in the digital control block to control a counter, and it also sets the ADC conversion time. This clock can be generated locally in the pixel or in the periphery of the pixel array and then distributed to all pixels. In our case the clock is assumed to be external to the pixel array and distributed to

all pixels. The two digital outputs are the *finished* signal and the N-bit *digital output*. *Finished* is used to notify the front-end and readout circuitry that a conversion has finished. It resets the hold capacitor shown in figure 5.12 and starts the readout sequence of the pixel data.

The design of the DAC is relatively simple thanks to the small required conversion time and bit resolution and it's explained in section 6.3.1. The most critical component in the ADC is the comparator. There is a direct relation between the power consumed by the comparator and the speed of the comparison, and this has a very direct influence on the linearity characteristics of the ADC. The comparator used is the same one described in section 5.2.1 and thus will not be explained in this chapter.

For a conversion time of one microsecond and a resolution of four bits, the digital circuitry in the ADC will have to work at a frequency of at least 4 MHz, and thus the design of the digital control block should not pose any problem. The digital block is explained in 6.3.2.

6.3.1 The digital-to-analog converter

The digital-to-analog converter (DAC) uses a binary-weighted current steering architecture as shown in figure 6.2.

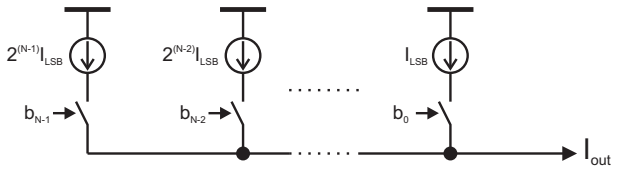

Figure 6.2: Basic block diagram of a current steering DAC.

An N-bit binary-weighted current steering DAC consists of an array of $2^N - 1$ unity current sources, each one with a value of I_{LSB}. The total output current from the converter can be expressed as:

$$I_{out} = \sum_{i=0}^{N-1} b_i \cdot 2^i \cdot I_{LSB} \tag{6.2}$$

where N is the number of bits, b_i is the digital binary value corresponding to bit i, and I_{LSB} is the value of the current for the basic current source.

The current sources corresponding to each bit are grouped together and connected to the output of the DAC via a switch controlled by the digital input to the DAC. Figure 6.3 shows the transistor implementation of the current source corresponding to bit i as the parallel connection of 2^i equal M_{LSB} transistors working as current sources.

Transistors M_{S1} and M_{S2} in the figure act as switches controlled by the digital input, and ensure that the current source is always operating independently of the digital value of its corresponding bit.

Using a first order approximation, and assuming that the transistors operate in saturation and strong inversion, we can obtain the aspect ratio W_{LSB}/L_{LSB}

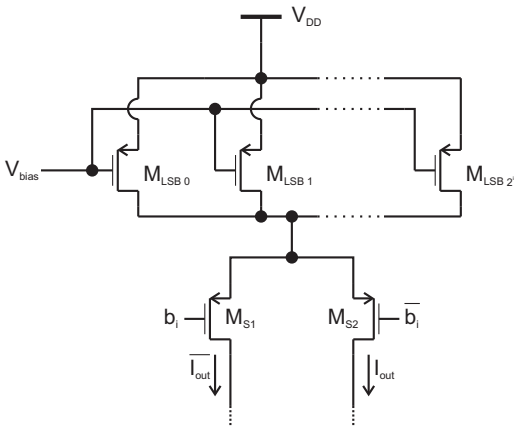

Figure 6.3: Transistor implementation of the current source corresponding to bit i.

of the unit transistor from:

$$\frac{W_{LSB}}{L_{LSB}} = \frac{2 \cdot I_{LSB}}{\mu_p C_{ox} \cdot (V_{bias} - V_{DD} - V_{TP})^2} \tag{6.3}$$

where μ_p is the mobility of the holes in the channel of the pMOS transistor, C_{ox} is the unit capacitance per area of the gate oxide, V_{bias} is the voltage applied to the gate of the transistor, V_{DD} is the positive supply voltage and V_{TP} is the threshold voltage of the pMOS transistor.

To determine the area of the transistor we can use the matching parameters of the technology and use the well known matching equations [2] to obtain:

$$W_{LSB} \cdot L_{LSB} = \left(2 \cdot \left(2^N - 1\right)\right)^2 \cdot \left(\frac{A_K^2}{K^2} + \frac{4 \cdot A_{VTO}^2}{(V_{GS} - V_{TH})^2}\right) \tag{6.4}$$

From Equations 6.3 and 6.4 we can determine the dimensions of transistor M_{LSB}. For our four-bit DAC and a full scale value of 1μA, the value for I_{LSB} is 62.5 nA. A value of 300 mV was chosen for the overdrive voltage of the transistor ($|V_{bias} - V_{DD} - V_{TP}|$). The final values for the width and length of the current source transistor are: $W = 420$ nm and $L = 10.48$ μm. The limitation was the value of W_{LSB}/L_{LSB} needed and not the matching requirement.

Figure 6.4 shows the layout of the DAC. To minimize the errors due to the geometrical placement of the current sources, a common-centroid geometry [3] was used for the layout of the current sources. To ensure good matching of the current sources, extra "dummy" transistors are added at both ends of the array. The size of the DAC including the switches is 19μm by 65μm.

The bias voltage V_{bias} in figure 6.3 is generated locally in each pixel. A bias current is sent to the pixels and the transistor marked as *mirror* in figure 6.4 generates the adequate gate voltage.

From the simulations performed on the DAC, it can be concluded that the DAC operates correctly up to a switching frequency of 100 MHz*, well above

*The switching frequency corresponds to the frequency of the digital signal applied to the

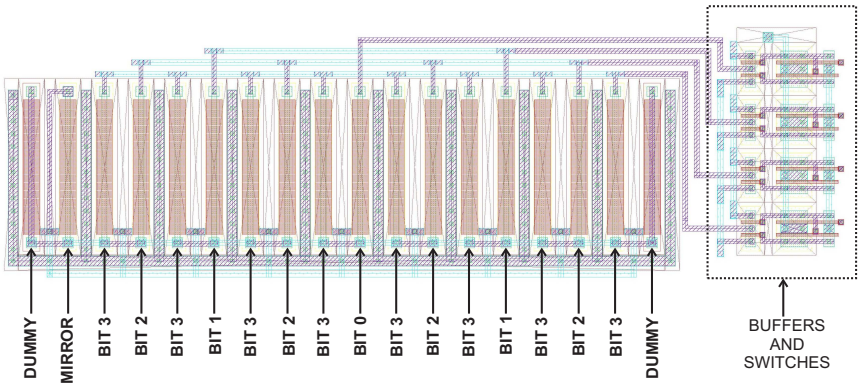

Figure 6.4: Layout of the DAC used in the successive approximation ADC, indicating to which current source belongs each transistor.

the original target of 4 MHz (corresponding to 1 μs conversion time and 4-bit resolution) with an error far below one half of an LSB without any kind of correction.

6.3.2 The digital control

The digital control block controls the output of the DAC based on the output of the comparator. Figure 6.5 shows a block diagram of this block. It consists of a two-bit counter, a two-to-four bit decoder, an additional logic block and a four-bit register. The two-bit *counter* is a synchronous Gray-code counter. The two-to-four bit *decoder* generates from the counter outputs the four different signals (one for each bit) that will be used in the register block to control the DAC.

As explained in chapter 4, all pixels (and hence all ADCs) in the pixel array will function independently of one another. This simplifies the distribution of the clock signal from the periphery to the pixels as the phase relationship of the clock in one pixel with respect to the other pixels is irrelevant.

The *event* input signal is generated by the hit detection block. The *comparator output* signal is the output of the comparator shown in figure 6.1. Both the *reset* and *clock* input signals are common to all pixels in the chip and are buffered locally in each pixel.

The *additional logic* block in figure 6.5 generates the *finished* output signal and two internal signals: *ResetADC* and *enable*. *ResetADC* is used to set the internal registers of the ADC to a known state when a global reset is being performed in the chip or while the converter is inactive (no photon hit has been detected). *Enable* controls the counter so that it starts counting when the hit detector detects a photon interaction and stops when the conversion has finished.

switches.

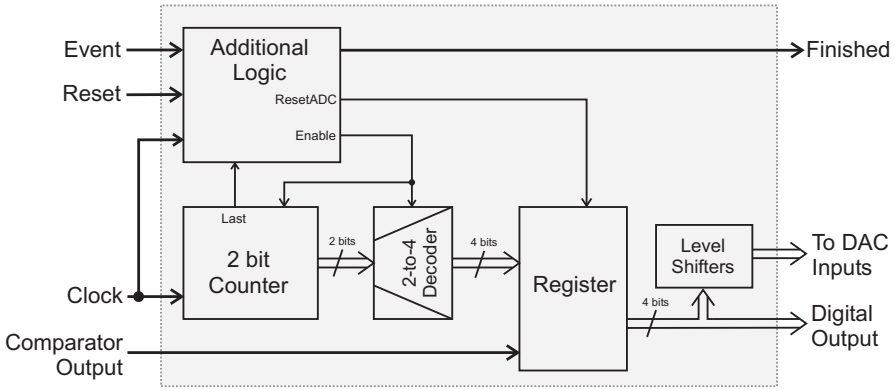

Figure 6.5: Block diagram of the digital control for the successive approximation ADC.

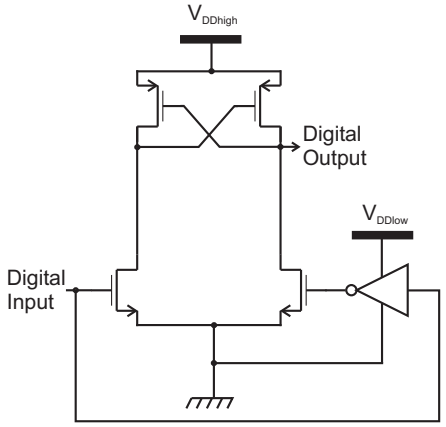

Figure 6.6: Schematic drawing of a level shifter used for the signals controlling the DAC switches.

The *register block* in figure 6.5 uses the output of the comparator to control the current sources in the DAC depending on the state of the counter. When the conversion has finished, the register stores the digital value.

In order to use the four-transistor comparator shown in figure 5.8, the positive supply voltage value for the comparator and the digital control block of the ADC is set to 1 V. The supply voltage of the DAC is kept at the higher value of 1.8 V in order to simplify the design of the current sources. This difference in power supply domains causes a problem in the generation of the signals controlling the switches in the DAC. To solve this problem the *level shifters* are used between the digital outputs of the digital control block and the DAC inputs. Figure 6.6 shows the schematic of a level shifter.

The digital circuitry worked correctly in simulations up to a clock frequency of approximately 250 MHz which is far beyond the specified operating frequency

of 4 MHz.

6.3.3 Simulations

Simulations of the ADC* showed the trade-off existing between the the speed of the comparator and the overall power consumption. Linearity errors appear when the current entering the comparator is smallest and, consequentely, the comparator needs a longer time to make a decision. Increasing the full scale current of the ADC would lead to a lower error at the expense of higher current consumption.

In order to check the overall performance of the ADC, the typical figure of merit (F.O.M.) of energy per conversion [1] is used. This number is calculated using Equation 6.1. The simulated average power consumption and the value of energy per conversion for the successive approximation ADC are summarized in table 6.2. The power consumption includes the power consumed by the peak and hold circuit from section 5.3.

Table 6.2: Power consumption and energy per conversion for the successive approximation ADC.

	Value	Unit
Power consumption (average)	14.965	μW
Energy per conversion	0.93531	pJ

The value of energy per conversion for this design compares favorably with state of the art Nyquist ADC designs, where typical values for the FOM range between 1 and 10 pJ per conversion [5].

6.3.4 Layout

Figure 6.7 shows the layout of the successive approximation ADC. The circuit occupies an area of approximately 85 μm by 85 μm. The digital outputs are located at the rightmost side and the analog data enters the circuit on the leftmost side. The DAC is clearly visible on the left side, with the comparator located at the top-left side and the digital circuitry occupying more than two thirds of the area on the right side.

All analog signals (input as well as bias) enter the circuit via the leftmost side. The input digital signals (*Reset*, *Clock*, *Event* and the output of the comparator) are routed between the analog and the digital blocks. The digital outputs are routed and connected to the *control and data bus* shown earlier in figure 4.6 at the rightmost side of the circuit. Metals 1 and 2 are used as much as possible for routing. Metal 3 is used for power supply routing and, in some cases, also for signal routing in order to keep the area as small as possible†.

*To simulate the operation of the ADC, multiple transient simulations have to be performed with changes in the input current. To perform these simulations with as many points as needed without heavily loading the computers, a piece of software was developed to simplify parametric simulations in hSpice [4].

†Although the technology allows for six metals, the multi-project wafers used only three metals.

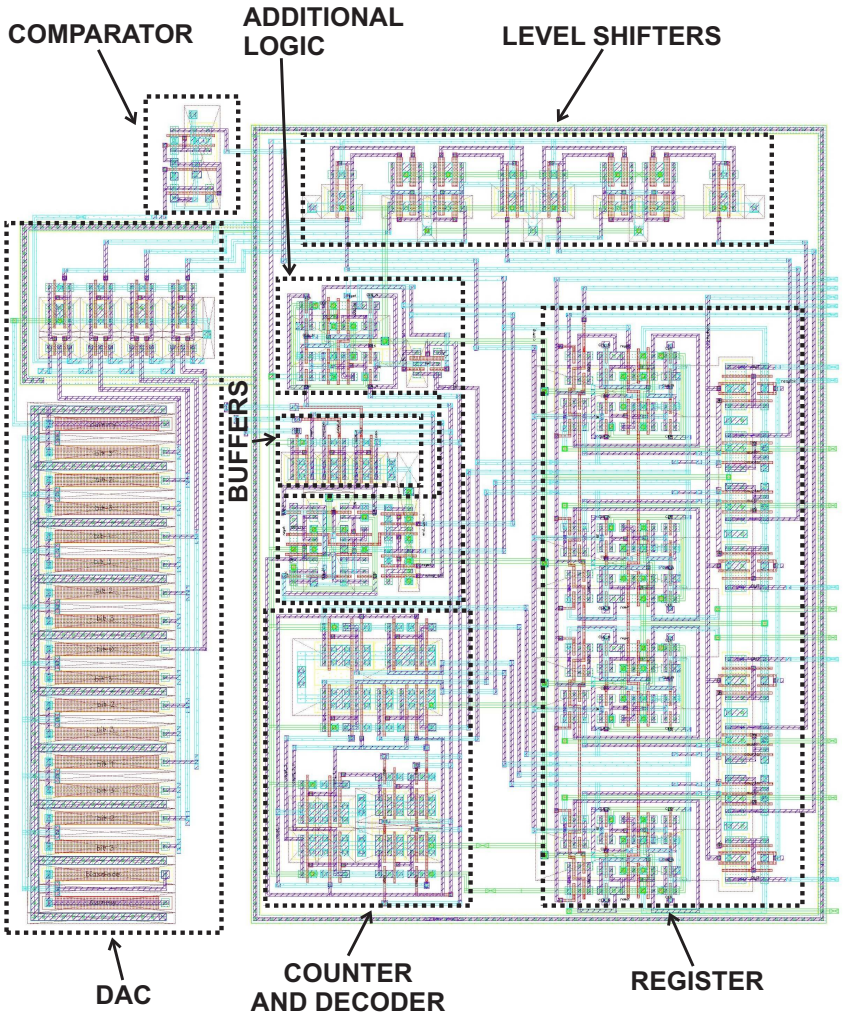

Figure 6.7: Layout of the successive approximation ADC.

6.3.5 Experimental results

When it comes to test the functionality of an ADC, there is plenty of literature available describing different methods to characterize and model the operation of the converters [6, 7, 8, 9, 10, 11]. Although the ADCs designed in our work should work at a relatively high speed, their input signal can be considered as DC, given that the *sample-and-hold* function is performed in the front-end electronics described in chapter 5. For this reason, the ADCs are characterized by using a DC signal as input, and controlling the conversion time.

Figure 6.8 shows the set-up used for the measurements of the successive approximation ADC. Figure 6.9 shows a photograph of the measurement set-up.

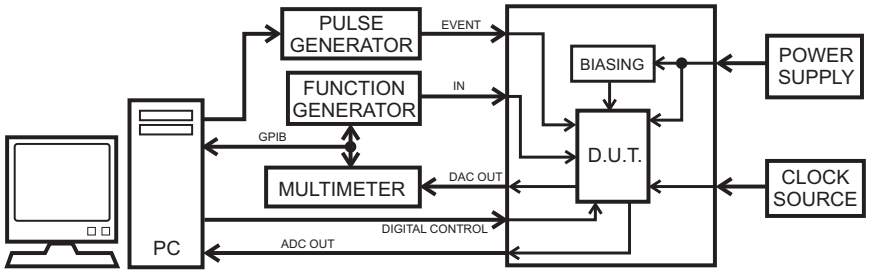

Figure 6.8: Set-up for the measurements of the successive approximation ADC.

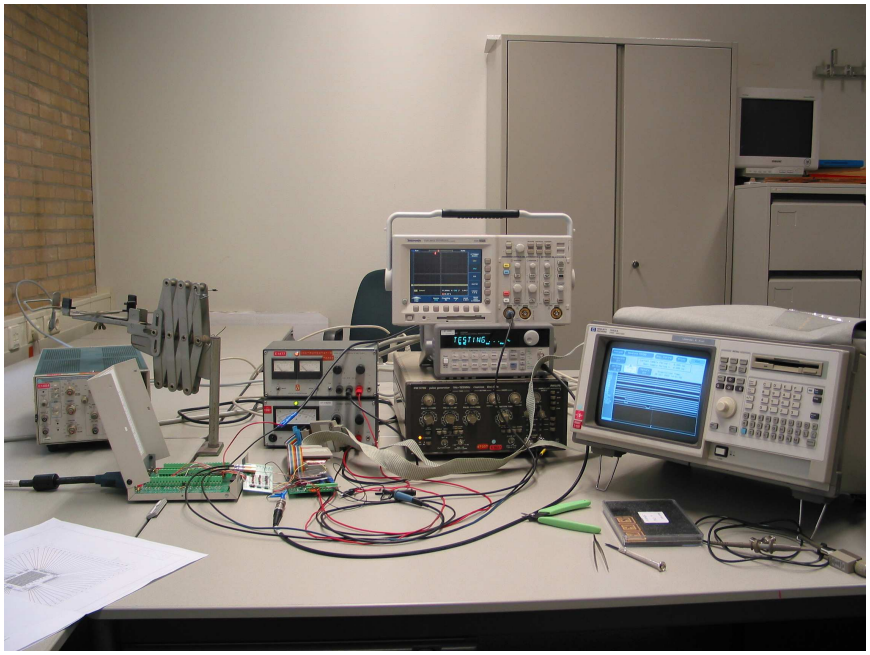

Figure 6.9: Photograph of the measurement set-up.

The *device under test* (D.U.T.) is placed in a custom designed printed circuit board which also includes the circuitry needed to bias the circuit and the necessary connectors to the instruments. A multi-functional I/O board* inside a conventional PC is used to generate the necessary digital signals, to capture the output of the ADC and to control the pulse generator that sends the *Event* signal. The PC uses the GPIB bus to control the function generator providing the ADC input signal and a multimeter used to measure the complementary output ($\overline{I_{OUT}}$) of the DAC. An external clock source is used to generate the clock for the ADC.

Figures 6.10 and 6.11 show, respectively, comparison of the measured and

*National Instruments PCI-1200.

simulated INL and DNL of the ADC for a conversion time of 1 μs and a power supply value of 1.8 V.

Five devices were measured. Only the results from one of them is shown as the variations between the five samples were very small. The operation of the ADC did not degrade much up to a conversion time of 200 ns (corresponding to a sample rate of 5 MSamples/s).

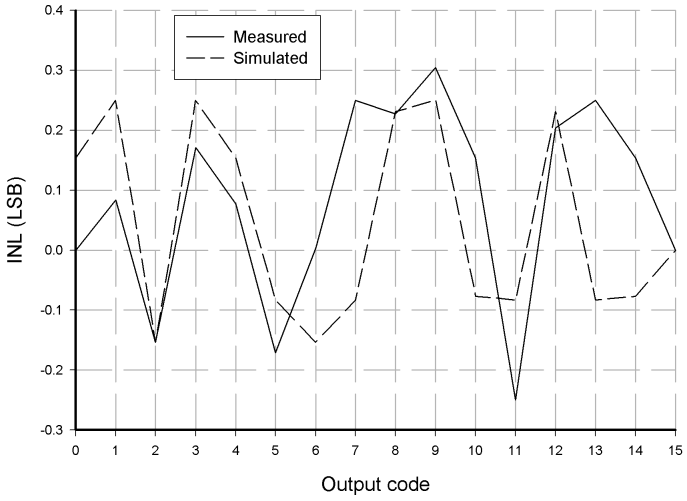

Figure 6.10: Comparison of the measured and simulated INL of the successive approximation ADC in the pixADC2 prototype chip.

The linearity shown in this figure, as well as for the algorithmic ADC is the deterministic one. As has been explained earlier in this thesis, the speed of the comparators depend on the level of the signal. There is, thus, a relation between conversion time and LSB current. The simulated values show the linearity of the ADC for the designed LDB current and speed. Shorter conversion time and/or smaller LSB current would lead to higher non-linearity. Considering that there was plenty of margin added for mismatch in the DAC current sources, the mismatch effect is barely seen in the measurements.

6.4 Algorithmic ADC

An algorithmic or cyclic ADC, like the successive approximation ADC, needs N comparisons for an N bit conversion. But instead of trying to approximate the input value with a DAC, it tries to approximate the full scale value by operating on the input value. If implemented as a *cyclic* ADC, each comparison is made at a different moment in time, but using the same comparator each time [12]. This implementation requires the use of non-overlapping digital signals to control

several switches. The circuit implemented here [13, 14], on the other hand, uses N different one-bit conversion blocks connected in cascade, which effectively results in a similar structure to a pipeline ADC. The biggest advantage of this particular implementation is that no digital circuitry is needed for the operation of the ADC, with the obvious exception of the memory blocks needed to store the output digital values.

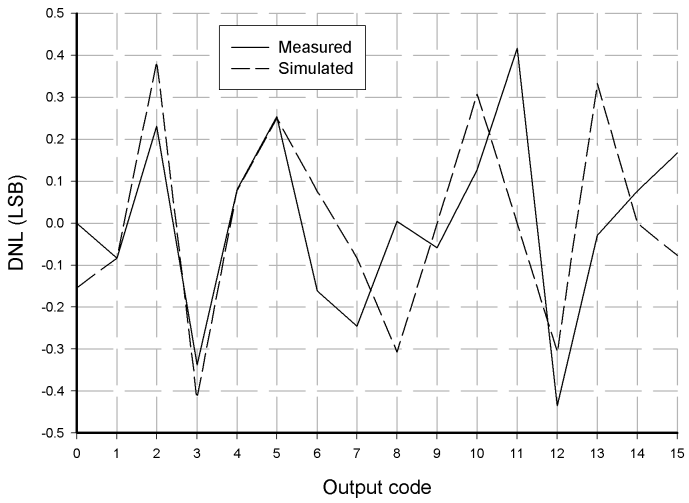

Figure 6.11: Comparison of the measured and simulated DNL of the successive approximation ADC in the pixADC2 prototype chip.

Figure 6.12 shows a block diagram of the algorithmic ADC. The converter consists of three main blocks. The *Analog block* performs the conversion as explained later in this section. It generates four digital outputs from the analog input. The *Delay* block generates two signals by delaying its *Event* input. One is used to latch the outputs of the digital blocks into the output register, and the other (*Finished*) indicates to the readout block that the conversion has finished. *Event* is typically the output of the hit detector and the delay is controlled by a *Delay control* signal. The *Latches* receive the digital output of the analog block and store it when the *Latch* output from the delay block changes value from low to high.

The delay block is implemented as a simple current-starved buffer sized for a mean delay of one microsecond. The latches are implemented as conventional D flip-flops.

Figure 6.13 shows the connection of the N one-bit conversion blocks which make up the *Analog block* in figure 6.12, as well as the latches.

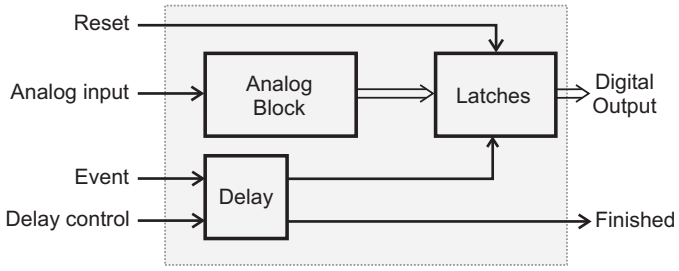

Figure 6.12: Block diagram of the algorithmic ADC.

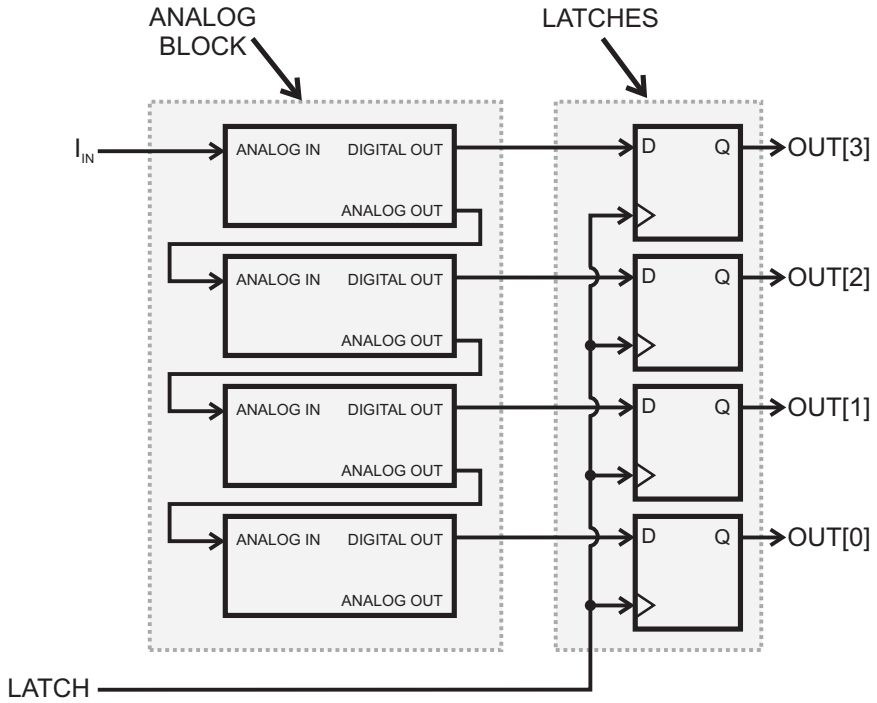

Figure 6.13: Connections between the analog and the digital part (latches) of the 4-bit algorithmic ADC.

The analog output of each bit block is used as input for the following bit block. The digital outputs of all blocks are sampled at the same time by the *latch* signal and are stored in the flip-flops.

Figure 6.14 shows the implementations of a one-bit conversion cell with an nMOS current mirror.

The input current I_{IN} is copied using the current mirrors $M_{N1} - M_{N2}$ and $M_{N1} - M_{N4}$. The aspect ratio W/L of transistors M_{N2} and M_{N4} is twice that of transistor M_{N1} so that the value of the current flowing through M_{N2} and M_{N4} is twice the value of the input current. Transistor M_{P3} works as a current source with a value equal to the full range of the ADC ($I_{FS} = 2^N \cdot I_{LSB}$). The difference between the currents flowing through M_{N2} and M_{P3} will enter the

current comparator:

$$I_{COMP} = I_{FS} - 2 \cdot I_{IN} \tag{6.5}$$

If $I_{COMP} > 0$, the digital output is set low and the drain of transistor M_{N4} is connected to the analog output. The output current is then equal to:

$$I_{OUT} = 2 \cdot I_{IN} \tag{6.6}$$

If $I_{COMP} < 0$, the digital output is set high and the analog output is equal to:

$$I_{OUT} = 2 \cdot I_{IN} - I_{FS} \tag{6.7}$$

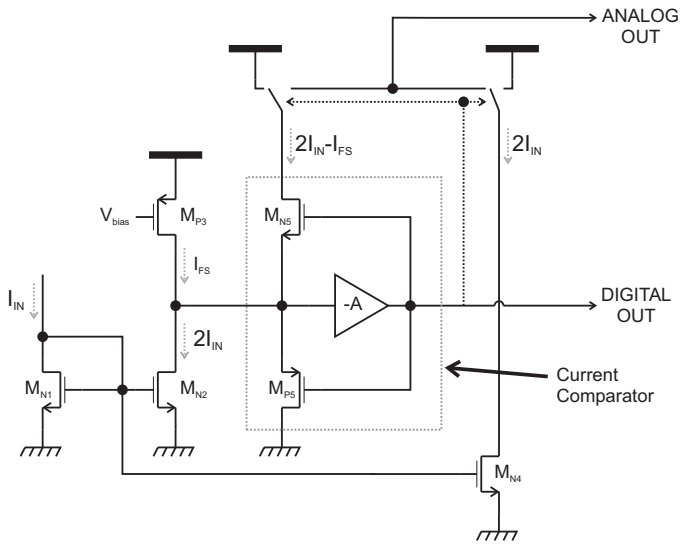

Figure 6.14: Bit-block implementing a one bit conversion in an algorithmic ADC with an nMOS input mirror.

In this last case, this current is already flowing through transistor M_{N5}. Thus, the drain of transistor M_{N5} is connected to the analog output.

It is clear from figure 6.14 that the analog output cannot be connected to the input of an identical one-bit block without using an intermediate current mirror. To avoid using an extra current mirror for each block, we use alternatively blocks such as the one in figure 6.14 and blocks like the one shown in figure 6.15.

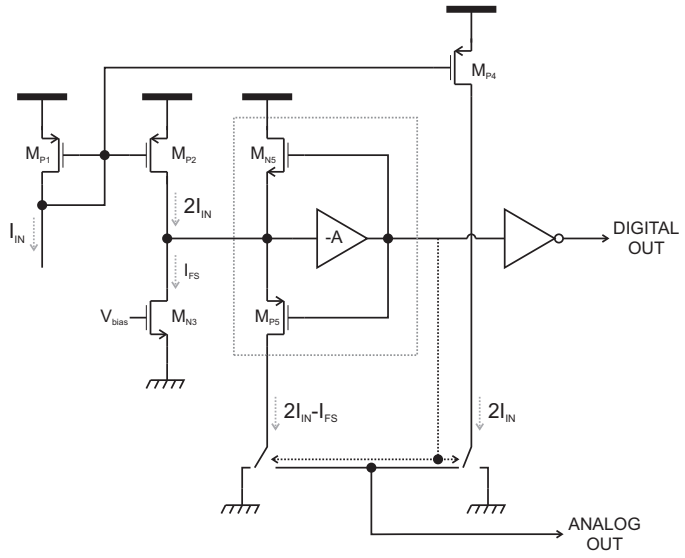

Figure 6.15: Bit-block implementing a one bit conversion in an algorithmic ADC with a pMOS input mirror.

The accuracy of this ADC depends on how good the current sources M_{P3} and M_{N3} as well as the current mirrors $M_{N1} - M_{N2}$, $M_{N1} - M_{N4}$, $M_{P1} - M_{P2}$ and $M_{P1} - M_{P4}$ are. The sizes of these transistors are calculated for good matching between the different one-bit blocks and to handle a full scale current of 1 μA. The design values are shown in table 6.3.

Table 6.3: Sizes of the transistors in the circuits shown in figures 6.14 and 6.15

Transistor name	Width (μm)	Length (μm)
M_{N1}, M_{N2}, M_{N3}, M_{N4}	0.8	5
M_{P1}, M_{P2}, M_{P3}, M_{P4}	0.8	1.5

6.4.1 The comparator

As figures 6.14 and 6.15 show, the same comparator used in the hit detection block and the successive approximation ADC is used in each bit-block of the algorithmic ADC *.

However, due to the voltage requirements in the current mirrors, the implementation shown in figure 5.8 cannot be used here, as it would consume too much current. A different implementation is used where the amplifier is implemented as a conventional common source and a voltage source is added between the output of the amplifier and the gate of one of the feedback transistors. To further reduce the power consumption in the amplifier, a low bias current is used together with a level-shifter (source-follower) at the input of the amplifier to match the gate-source voltage of the amplifying transistor to its low bias

*The implementation of this comparator as well as the reuse of the current is the main difference between this design and the one reported in [13] and [14]

current. All this can be seen in figure 6.16.

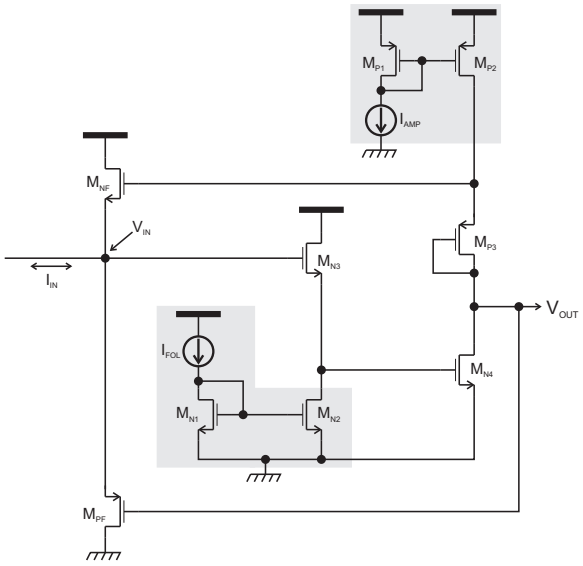

Figure 6.16: Implementation of the comparator in the algorithmic ADC. The bias networks are shaded in grey. Transistors M_{P1} and M_{N1} are common to the four comparators.

Transistors M_{NF} and M_{PF} have the same function as transistors M_N and M_P in figure 5.7. Transistors M_{N3}, M_{N2} and M_{N1}, as well as the current source I_{FOL} form the source-follower. Transistors M_{N4}, M_{P1} and M_{P2} and current source I_{AMP} form the common-source amplifier. Transistor M_{P3} works as a voltage source and it is used to bring M_{NF} into conduction faster by boosting the output voltage of the amplifier and thus increasing the gate-source voltage of transistor M_{NF}.

6.4.2 Simulations

The values of average power consumption and energy per conversion are summarized in table 6.4. In this case the energy per conversion is about 50% worse than for the successive approximation ADC, in part due to the bias needed for the comparator, which increases the static power consumption. As with the successive approximation earlier, the power consumed by the peak and hold circuit from section 5.3 is also included in the calculation.

Table 6.4: Power consumption and energy per conversion for the algorithmic ADC.

	Value	Unit
Power consumption (average)	21.79	μW
Energy per conversion	1.362	pJ

6.4.3 Layout

In the layout of the ADC all nMOS and all pMOS transistors for the different one-bit blocks were laid out together to improve the matching, with "dummy" transistors added at the edges. Figure 6.17 shows the layout of the ADC in the prototype chip.

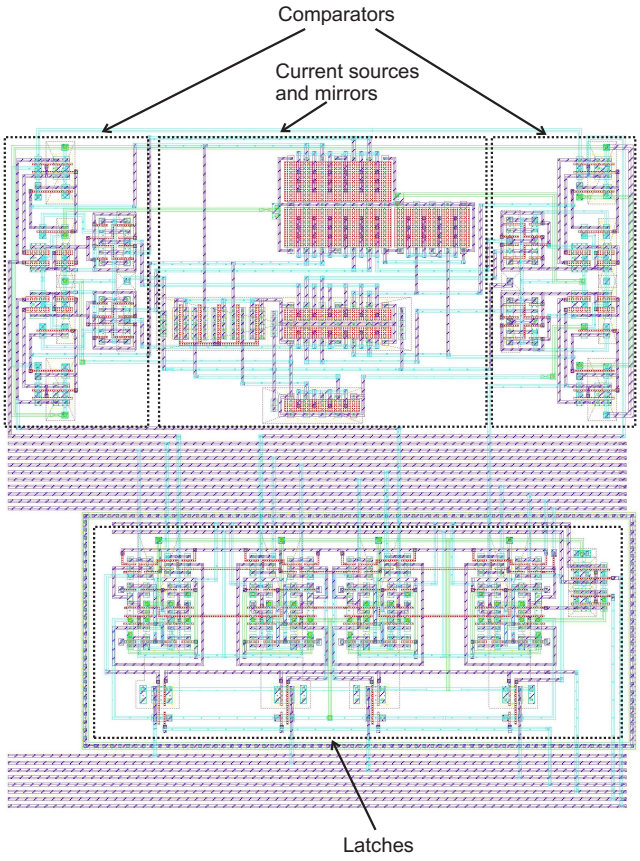

Figure 6.17: Layout of the algorithmic analog-to-digital converter.

6.4.4 Experimental results

Figure 6.18 shows graphically the set-up used to characterize the algorithmic ADC. This set-up is simpler than the one shown in figure 6.8 as there is no clock source needed.

The same multi-functional I/O board used in the characterization of the successive approximation is also used for the characterization of the algorithmic ADC. A function generator is controlled by the PC via the GPIB bus to generate the input to the ADC, and a pulse generator controlled by one of the digital

outputs of the I/O board is used to generate the *Event* signal which is delayed to latch the digital values of the one-bit blocks of the ADC into the register. The conversion time is controlled by the delay between the *Event* input and *Latch* output.

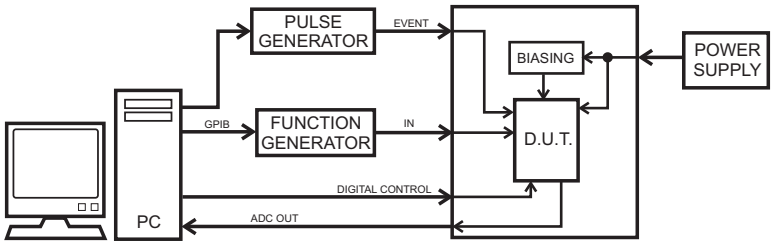

Figure 6.18: Set-up for the measurements of the algorithmic ADC.

In order to characterize the ADC with more detail, the delay block is overridden and the latch signal is generated externally to control better the conversion time during evaluation. Figure 6.19 shows how the conversion time is controlled.

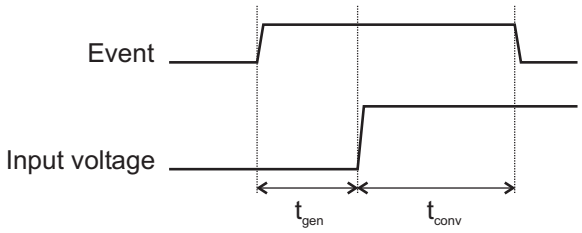

Figure 6.19: Control of the conversion time for the algorithmic ADC.

The *event* signal is used to trigger the signal generator. The time from the rising edge of *event* to an update of the output of the generator (t_{gen}) is known from the specifications of the instrument and can be measured to adjust the overall timing precision. When *event* falls, the ADC is latched. The conversion time (t_{conv}) is fixed by the width of the *event* signal, and can also be monitored and measured if additional accuracy is needed.

Figure 6.20 shows a comparison of the measured and simulated INL of the algorithmic ADC in one device, and figure 6.21 shows the same comparison for the DNL. As with the successive approximation five devices were measured and all of them had very similar results.

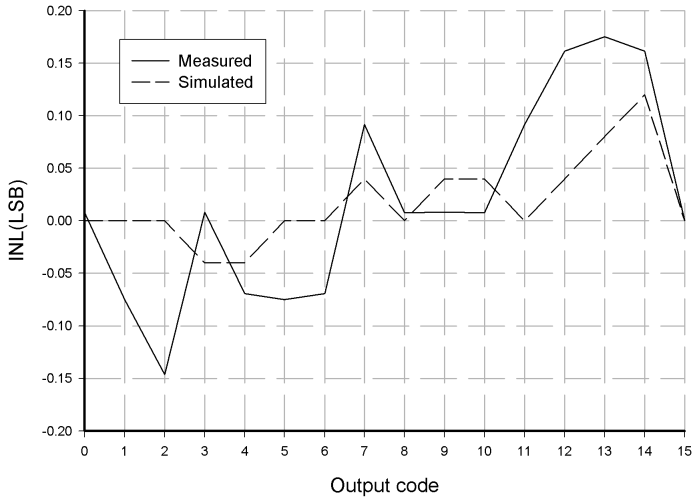

Figure 6.20: Comparison of the measured and simulated INL of the algorithmic ADC.

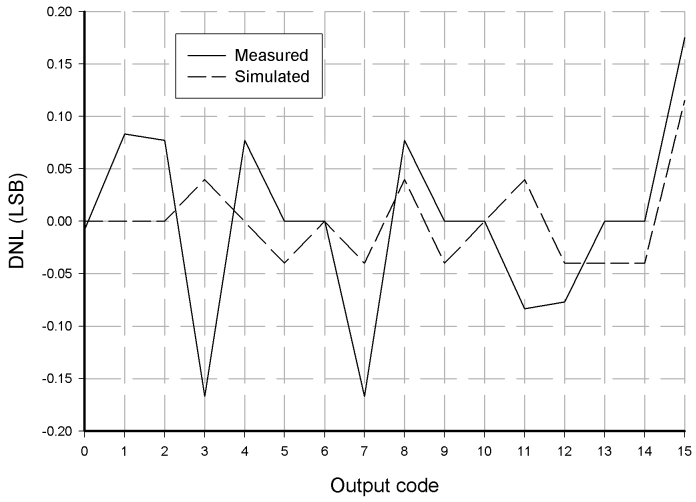

Figure 6.21: Comparison of the measured and simulated DNL of the algorithmic ADC.

6.5 ADC comparison

The successive approximation ADC seems to be the most complex circuit, as it requires a digital control of a set of current sources depending on a comparison made between the output of the current sources and the input signal to the ADC. However, this control is made almost entirely in the digital domain. This assures uniformity in the behavior of the circuit across the pixel array. The only constraint in the design is to assure maximum matching between the current sources used in the ADCs across the array. The algorithmic ADC, on the other hand, does all its processing in the analog domain. Although the operations are relatively simple, it is much more prone to differences in operation due to changes in operating conditions (temperature, supply voltages, etc.) and it is more difficult to achieve uniformity in the response across the pixel array.

Uniformity in the response of the ADCs is to a certain extent very much dependent on the amount of bias values needed to operate the ADCs (see Appendix A). In that respect the successive approximation ADC has a clear advantage in that it only needs one bias value (for the current sources in the DAC), while the algorithmic ADC needs at least one for the current sources and two for the comparator.

In terms of power consumption it might be better to use the energy spent per conversion than the power consumption of the converter itself. In that respect the successive approximation has a somewhat smaller value of $8.8 \cdot 10^{-13}$ J vs $1.3 \cdot 10^{-12}$ J for the algorithmic ADC. But it is worth remembering that this value only counts when the ADC is performing a conversion. From the system considerations laid out in chapter 4 it is clear that the ADCs will not be working continuously, but only when a photon interaction has taken place. In that respect it is important to compare the power consumed when the ADC is not active. The successive approximation needs a current of 1 μA for the DAC, while the algorithmic needs at least 1 μA for each bit plus the bias currents needed for each comparator.

The fact that the circuitry of the successive approximation is mostly digital makes its controllability and testability much easier, as well known digital testing techniques can be used to test the functionality of most of the ADC's functional blocks. The "analog" nature of the algorithmic ADC makes its testability and controllability more difficult.

A very important issue regarding the ADCs presented in this chapter is *scalability*. Or in other words, how well does the ADC scale with new fabrication technologies, with number of bits and with occupied area. In this issue the successive approximation also rates better than the algorithmic again because of the *almost digital* nature of the ADC. The trend in CMOS technology is to scale the transistor geometry to include more digital functionality in the same area. A look at figures 6.7 and 6.17 shows that the ADC which would benefit more of this trend is the successive approximation ADC, as most of its area is taken by digital circuitry. Moreover, the scaling of the "analog" transistors does not follow the same trend, as matching and noise requirements limit the achievable reduction in area. Given that an increase in the number of bits would lead to an increase in the overall area of the ADC, it is clear that the successive approximation ADC presents a clear advantage over the algorithmic ADC.

The only issue where the algorithmic ADC can perform better than the successive approximation is in the noise induced by the activity of the circuitry.

Due to the nature of the successive approximation ADC, switching noise is generated in each ADC, meaning that the analog circuitry must be well isolated from the digital.

Taking all these considerations into account, the successive approximation was used to build the next prototype chip, where an array of pixels was built to test the readout circuitry, as will be explained in the following chapter.

Bibliography

[1] R.H. Walden. Analog-to-digital converter survey and analysis. *IEEE Journal on selected areas in communication*, 17(4):539–550, April 1999.

[2] M.J.M. Pelgrom et al. Matching properties of MOS transistors. *IEEE Journal of Solid-State Circuits*, 24(5):1433–1439, October 1989.

[3] C.A.A. Bastiaansen et al. A 10-b 40 MHz 0.8-um CMOS current-output D/A converter. *IEEE Journal of Solid-State Circuits*, 26(7):917–921, July 1991.

[4] http://www.nikhef.nl/user/dbello/txts/doctorat/perlparam.html.

[5] K. Philips. Continuous time sigma-delta adcs. In *CICC 2004 Educational Sessions*, 2004.

[6] G. Pretzl. Dynamic testing of high-speed A/D converters. *IEEE Journal of Solid-State Circuits*, SC-13(3):368–371, June 1978.

[7] J. Doernberg et al. Full-speed testing of A/D converters. *IEEE Journal of Solid-State Circuits*, SC-19(6):820–827, December 1984.

[8] M. Vanden Bossche et al. Dynamic testing and diagnostics of A/D converters. *IEEE Transactions on Circuits and Systems*, 33(8):775–785, 1986.

[9] IEEE Standard for Digitizing Waveform Recorders. Technical Report IEEE Std. 1057, December 1994.

[10] V. Liberali et al. Dynamic characterisation of A/D converters using fast Walsh transform. *Microelectronics Journal*, 31:83–90, 2000.

[11] A. Cruz Serra. A new measurement method for the static test of ADCs. *Computer Standards & Interfaces*, 22:149–156, 2000.

[12] J.-S. Wang et al. A 12-bit 100-ns/bit 1.9-mW CMOS Switched-Current Cyclic A/D Converter. *IEEE Transactions On Circuits And Systems-II: Analog and Digital Signal Processing*, 46(5):507–516, May 1999.

[13] D.G. Nairn and A.T. Salana. Current-mode algorithmic analog-to-digital converters. *IEEE Journal of Solid-State Circuits*, 25(4):997–1003, August 1990.

[14] G. Giustolisi et al. Resolution of a Current-Mode Algorithmic Analog-to-Digital Converter. *IEEE Transactions On Circuits And Systems-I: Fundamental Theory And Applications*, 49(10):1480–1486, October 2002.

Chapter 7

Digital data readout

This chapter describes in more detail the pixel array architecture introduced in section 4.2.2 and the circuits used to read the digital data from the pixels (i.e., ADC value, row and column address) for each photon interaction.

Section 7.1 explains the *token-bus* protocol used for selecting the pixel whose data will be read, as well as the most important signals involved in the operation of the readout system. Section 7.2 describes the circuitry used to read the ADC data from the pixels. Section 7.3 describes the tests done in the pixADC4 prototype chip, which included the readout architecture described in this chapter together with an array of pixels with the functionality described in the previous chapters. Finally, section 7.4 offers a summary of this chapter. A more detailed explanation of the implementation of the circuits explained in section 7.1 can be found in Appendix C.

7.1 Token-bus architecture

Section 4.2.2 introduced the architecture of the pixel array. This section will go in more detail in the implementation of the protocol used to select the pixel whose data will be read.

As mentioned in chapter 4 the pixel array is divided in blocks, each one consisting of two columns of pixels. Each two-column block has its own token circulating through the pixels. The control of the token circulation as well as the sensing of the pixel data is taken care of by a *column control and readout* circuit.

Figure 7.1 shows the connections in a *two-column block* between the pixels and the control circuit. The figure also shows the basic signals connecting the column control block to the rest of the readout circuitry which will be explained later in section 7.1.2.

The token circulation is controlled via the T_{IN}, T_{OUT}, W_{IN} and W_{OUT} signals*. The other signals going between the pixels and the column control circuit can be divided into *data* and *control* signals.

The data lines are the ADC output ($DATA$) and the pixel ROW address. Every pixel has its row address set as a read-only-memory (ROM) and when the pixel receives the token it puts this address in the ROW bus. The ADC

*W stands for *Wait*, while T stands for *Token*.

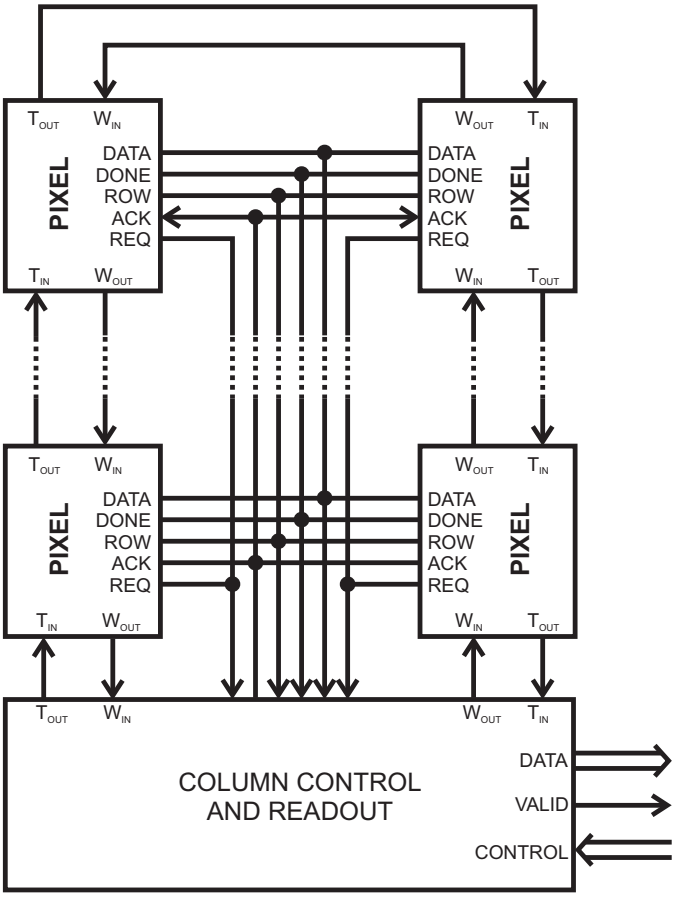

Figure 7.1: Block diagram of a two-column block, indicating the signals communicating the pixels and the peripheral control block.

output data bus is connected to the outputs of the ADCs of all the pixels in the two columns as explained later in section 7.2.

The control lines are *DONE*, *REQ* and *ACK*. *DONE* is the *finished* output of the ADC in the pixel as explained in chapter 6 and is used to indicate to the column block that the pixel has processed a photon interaction and that the token circulation can begin. The signals *ACK* and *REQ* are used to implement a handshake protocol between the pixel and the column control and readout circuit to transfer the data from the pixel. Each column has its own *REQ* connection because this signal is also used to determine to which one of the two columns belongs the pixel that has been read.

The token circulation is initiated when one or more pixels in any of the two columns have processed a photon interaction. The pixels notify the column control block by setting *DONE* high. The token signal will begin to flow from the column control block through its T_{OUTP} output to the first pixel in the first column. The token will continue to circulate from pixel to pixel via the T_{IN} input and T_{OUT} output in the pixels. When the token arrives at a pixel which has processed a photon interaction, this pixel will stop the token circulation and put its ADC data and its row address in the *DATA* and *ROW* buses respectively. At the same time it will send a request to the column block by setting *REQ* high to indicate that the data in the buses is valid. When the column block sees that one of its *REQ* inputs is high, it will read the contents of the *DATA* and *ROW* buses and it will indicate to the pixels that the data has been read by setting *ACK* high. When the pixel which had the token detects a rising edge in *ACK*, it will set its *DONE* and *REQ* outputs low and resume the token circulation to the next pixel.

Once the token reaches the last (upper) pixel in the column, it must return to the column block to close the ring. If the last pixel in the first column is connected directly to the column block, the distance from the pixel to the column block will be very large and either the pixel needs to spend more power to drive the long interconnect line or a long delay will exist between the token output of the pixel and the token input of the column block. The solution chosen in the system described in this thesis is to connect the last pixel in the first column to the pixel next to it in the contiguous column. From here the token circulates downwards until it reaches the column block. This is the main reason for choosing blocks of two columns for the token circulation*. When the token reaches the column block the token circulation will be stopped if none of the pixels in the two columns has processed an interaction (i.e. the *DONE* input of the column block is low) or if the data from the pixels which had processed an interaction has been read.

The pixel receives the token signal through its T_{IN} input from the previous pixel in the token ring and sends to the same previous pixel the signal W_{OUT}. W_{OUT} indicates that the pixel has data to be read by the column block in the periphery, and it will be used in the control of the token signal being passed between the pixels. The pixel also sends the token signal to the next pixel through T_{OUT} and receives the wait signal W_{IN} from that same next pixel. The token and wait inputs and outputs are controlled by the *BYPASS* signal as shown in figure 7.2.

*This basic architecture can easily be extended to any even-numbered column-blocks if needed.

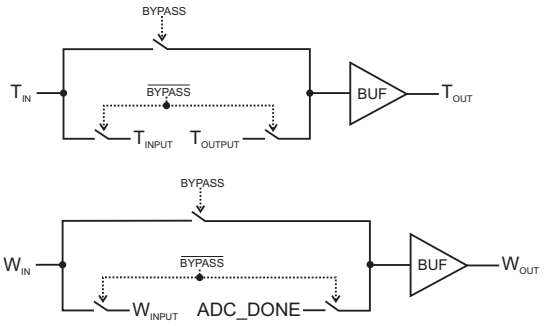

Figure 7.2: Circuitry used to bypass the pixel for readout.

In the figure, T_{IN}, T_{OUT}, W_{IN} and W_{OUT} represent the inputs and outputs of the pixel blocks shown in figure 7.1. The signals T_{INPUT}, T_{OUTPUT} and W_{INPUT} are the internal signals of the pixel readout block that will be used in the circuitry described next in section 7.1.1.

The *BYPASS* signal is set in the pixel configuration block mentioned in section 4.2.1 and is used to disable the pixel. This signal can be used, for example, to read only one section of the imaging array, to disable pixels not working properly or with a faulty bump bond to the sensor, etc. If the pixel is set to be bypassed the token is sent directly to the following pixel in the column block as soon as it arrives to the pixel.

Section 7.1.1 explains the circuitry needed in the pixel to implement the protocol described above. Sections 7.1.2 and 7.1.3 describe, respectively, the column block and how the column blocks are connected together.

7.1.1 Pixel circuitry

The circuitry located in the pixel in charge of handling the token circulation has been designed as an *asynchronous sequential circuit*. In it, only logic gates are used instead of latches to implement the sequential nature of the circuit. This approach leads to a simplified design in terms of number of transistors, and thus in occupied pixel area.

From the point of view of the token circulation, a pixel can be found in one of two possible states. In the first state the processing electronics in the pixel have processed a photon interaction and the pixel has data that needs to be read: the pixel is said to be *full*. In the second state the pixel has not processed a photon interaction and the pixel is *empty*.

Due to the asynchronous nature of the token circulation, the state of the following pixel in the token flow is important for the correct circulation of the token. Four possible states can be defined in which two consecutive pixels can be found depending on whether a pixel has processed a photon interaction or not at the moment when a token arrives to its T_{IN} input. These states are summarized in the Table 7.1.

In the first state the pixel receiving the token has not processed (or finished processing) a photon interaction when the token arrives at its input, and neither has the following pixel. In this case the pixel has no data to send and the token is simply passed on to the next pixel.

Table 7.1: Pixel states.

State	Pixel	Following pixel
1	Empty	Empty
2	Full	Empty
3	Empty	Full
4	Full	Full

Figure 7.3 shows a timing diagram with the relevant signals.

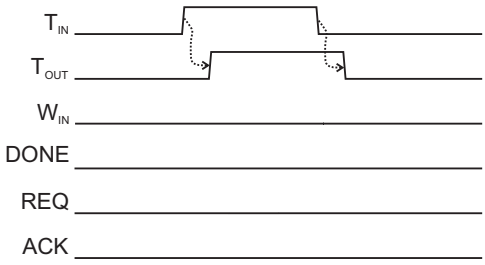

Figure 7.3: Timing diagram of the signals in a pixel when the pixel was not hit and the following pixel was also not hit.

If the pixel receiving the token has not processed a photon interaction the signal *done* will be low at a rising edge of T_{IN} *. If the W_{IN} input is low the next pixel in the token chain has not processed a photon interaction either. When these two conditions are fulfilled the input token is passed directly to the the next pixel.

The second state occurs when the pixel receiving the token has processed a photon interaction before the rising edge of the input token (*done* is high), and the next pixel has not processed a photon interaction (W_{IN} is low). The timing diagram corresponding to this state is shown in figure 7.4. The output token must only go high after the pixel data has been read from the pixel.

When the pixel senses a rising edge in its T_{IN} input, the pixel takes control of the internal *data* and *row* buses and stops the token circulation if *done* is high. At the same time it begins the handshake communication with the column block by raising *req*. The answer of the column block by setting *ack* high tells the pixel that the data (ADC output and row address) has been read, and hence it can put both *done* and *req* low†. When the column block sees a falling edge of *req* it sets *ack* also low to signal that the communication has ended. When the pixel detects that *ack* has gone low, it resumes the token circulation by setting T_{OUT} high.

*Note that the ADC might be processing a photon interaction at this point, but the circuit will only react to the level of *done* at the rising edge of T_{IN}. If a photon interaction was being processed, the pixel will have to wait to the next time that the token enters the pixel. This behavior can be modified for example by using the output of the comparator instead of the *DONE* signal, but then additional circuitry should be added to start the data communication only when the analog-to-digital conversion has ended (i.e. *done* is high).

†By keeping *done* high until the data has been read, the ADC is effectively blocked and cannot process more photon interactions.

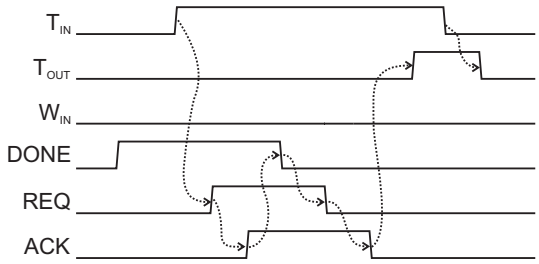

Figure 7.4: Timing diagram of the signals in a pixel when the pixel was hit but the following pixel was not hit.

The timing diagram corresponding to the third state is shown in figure 7.5.

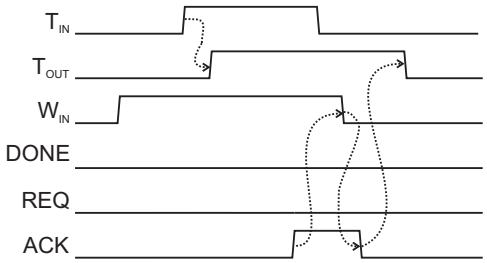

Figure 7.5: Timing diagram of the signals in a pixel when the pixel was not hit but the following pixel was hit.

In this state the pixel receiving the token has not processed a photon interaction at the time the input token goes high. However, the following pixel has processed a photon interaction, indicated by W_{IN} being high at the rising edge of T_{IN}. The pixel receiving the token must hold T_{OUT} high until the column block has signalled that the data from the following pixel has been read.

In the fourth and last state both pixels have processed a photon interaction, indicated by both *DONE* and W_{IN} being high in the pixel receiving the token when T_{IN} goes high. The corresponding timing diagram is shown in figure 7.6.

The difference to the second state explained earlier is that now T_{OUT} will only go low after W_{IN} and ACK have gone low (as in the third state). In other words, the output token will go high when the data of the pixel has been read and it will go low again when the data from the following pixel has also been read.

7.1.1.1 Transistor implementation

To implement the token handling circuitry as an asynchronous sequential circuit a logic gate called *C element* [1] is used. The token handling circuitry implemented uses a C element with one input connected to the token signal coming from the previous pixel (T_{IN}) and the other input connected to an internal signal called B_{IN}. The output of the C element is the token signal going to the following pixel (T_{OUT}).

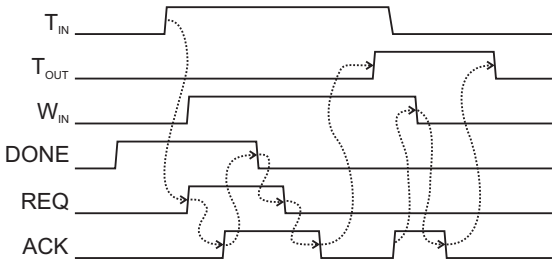

Figure 7.6: Timing diagram of the signals in a pixel when both the pixel and the following pixel were hit.

The internal signal B_{IN} is derived using the signals *done*, T_{OUT}, W_{IN} and *ack* according to figures 7.3 to 7.6. Table 7.2 shows the truth table used to derive B_{IN}.

Table 7.2: Derivation of the B_{IN} signal using the timing diagrams in figures 7.3, 7.4, 7.5 and 7.6

done	T_{OUT}	W_{IN}	*ack*	B_{IN}
0	0	0	0	1
0	0	0	1	0
0	0	1	0	1
0	0	1	1	0
0	1	0	0	0
0	1	0	1	1
0	1	1	0	1
0	1	1	1	1
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	0
1	1	0	0	0
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1

The resulting logic equation is:

$$B_{IN} = \overline{\overline{(\overline{DONE} \cdot \overline{T_{OUT}} \cdot \overline{ACK})} \cdot \overline{(T_{OUT} \cdot \overline{W_{IN}} \cdot ACK)} \cdot \overline{(T_{OUT} \cdot W_{IN})}} \quad (7.1)$$

In the actual implementation, a delay is inserted between the token input and the equivalent signal applied to the input of the C element. This is done in order to take into account the inherent delay in the generation of the B_{IN} signal.

To simplify the circuitry needed in the pixels and in the periphery, the request signal is derived from the row address. The pixels' row addresses are encoded so that at least one bit has always a value of *one*. The *row sensing*

circuitry in the periphery generates the *req* signal by performing a logical OR of the row address bits.

7.1.2 Implementation of the column control block

Figure 7.7 shows how the column blocks are interconnected among themselves when all columns share one link to the external control and data acquisition system.

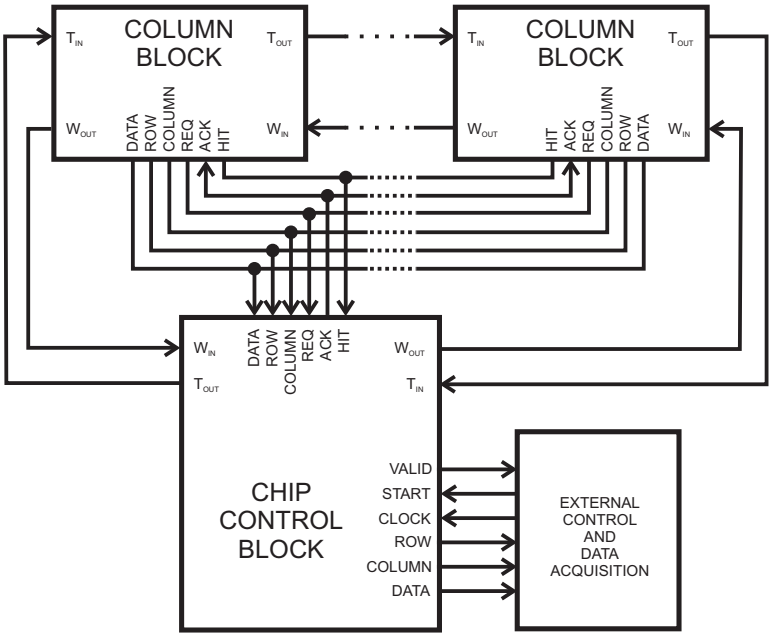

Figure 7.7: Block diagram showing the interconnections of the column control blocks and their interface to the external control and data acquisition system.

To simplify the design the same token bus protocol used in the pixels is used to select which column control block is selected to be read. A control block, called the *chip control block* is used to control the flow of the token and to interface to the external control and data acquisition system. The implementation of the chip block will be explained later in section 7.1.3.

As with the pixels, the column control blocks are connected to one another by *token* (T_{IN} and T_{OUT}) and *wait* (W_{IN} and W_{OUT}) signals. All column blocks share the common signals *DATA*, *ROW*, *COLUMN*, *HIT*, *REQ* and *ACK*, which are connected to the chip control block. The first three form the actual data that has to be read by the external system. The *HIT* signal serves the same purpose as *DONE* in the pixels. *REQ* and *ACK* implement the handshake communication between the column control blocks and the chip control block. In fact, the same timing diagrams shown in 7.3 to 7.6 can be drawn for the columns, exchanging *DONE* by *HIT*.

The external system provides the *START* and *CLOCK* signals to the chip control block. *START* is used to notify the column block that the external

system is ready to read data from the chip. *CLOCK* is used to control when the output data from the chip (*ROW*, *COLUMN* and *DATA*) is sampled by the external system. The *VALID* signal indicates that the data appearing in the *ROW*, *COLUMN* and *DATA* can be read*.

Figure 7.8 shows all the input and output signals of a column control block.

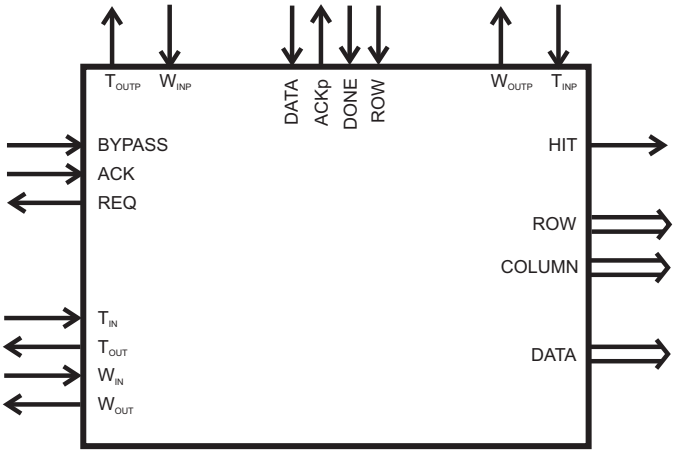

Figure 7.8: Input and output signals of a column block.

The signals shown at the upper side of the figure are the signals going to or coming from the pixels. The T_{OUT} output from the last pixel in the two column ring (T_{INP} in the figure) is connected to T_{IN} of the first pixel in the first column (T_{OUTP} in the figure) and W_{OUT} of the first pixel (W_{OUTP} in the figure) is connected to W_{IN} of the last pixel (W_{INP} in the figure). The signals REQ_0 and REQ_1 correspond to the *REQ* signal explained earlier in section 7.1.1 as well as to indicate to which of the two columns controlled by the column block belongs the pixel being read by controlling the last bit of the column address.

The four signals at the left side of the figure are the signals handling the token circulation between the different column control blocks.

The signals on the right side are the signals connecting each column control block to the chip control block. A *BYPASS* signal, analogous to the signal used in the pixels, is used to bypass one column block if needed. This could be done, for example, to limit the imaging area being read to only a part of the chip. The signals *ACK* and *REQ*† are used to implement a handshake communication protocol with the chip control block. The *HIT* signal indicates to the chip control block that a pixel belonging to one of the two columns controlled by the column control block has data ready to be read. The *DATA*, *ROW* and *COLUMN* signals are connected to the corresponding *chip-wide* buses, which

*If a handshake communication must be implemented with the external control and data acquisition system, the "Request" signal from the pixel readout chip would be the *VALID* output, while the "Acknowledge" signal from the external system would be the *CLOCK* signal.

†As mentioned earlier, the functionality of the *REQ* signal is implemented by the coding of the pixel *ROW* address.

in turn are connected to the corresponding chip outputs.

Figure 7.9 shows a block diagram of the circuitry in the column control block. Detailed schematics for the different sub-blocks can be found in Appendix C.

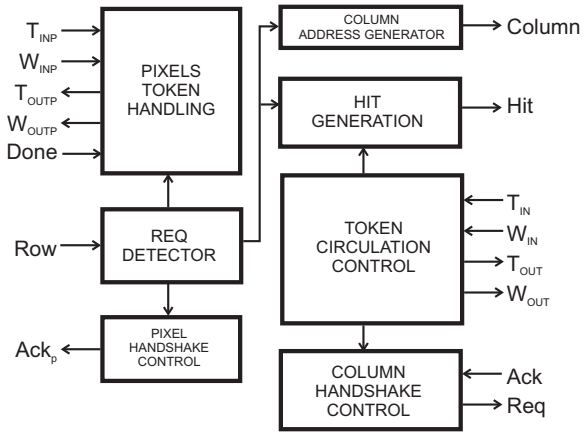

Figure 7.9: Block diagram of the implementation of the column block in figure 7.8.

The *Pixels Token Handling* block starts the token circulation when one or more of the pixels in any of the two columns has processed a photon interaction (indicated by *DONE* being high).

The *Row* address signal is read by the *req detector* block to generate the equivalent *Req* signal. The acknowledge signal sent to the pixels (Ack_p) is generated in the *Pixel handshake control*. The column address is generated in the same way as the row address for the pixels. A number of hardwired current sources are used in each column block. To distinguish between the two columns controlled by one column block, the *Row* address also includes one bit indicating to which column belongs the pixel. The last bit of the *Column* address is thus controlled by the *Row* signals sent from the pixels.

The same token bus architecture used in the pixels is used in the column blocks to control which one is allowed to transfer its data to the chip block. The equivalent for the columns of the column block for the pixels is the *chip block*. The *Hit* signal indicates that one of the pixels in one of the two columns belonging to the column block has sent a request to the column block. In this case the column block has valid data to transfer to the external data acquisition system. This *Hit* signal is used by the chip block in the same way as *Done* is handled by the column blocks. To control the data transfer between the column blocks and the chip block with the *Ack* and *Req* signals, a *column handshake control* block is used.

7.1.3 Implementation of the chip block

Figure 7.10 shows the inputs and outputs of the *chip block* shown in figure 7.7. This circuit is used to control the token passing through the columns and to interact with the external control and data acquisition system.

The *Columns token handling* block starts and stops the token circulation in the columns as the *Pixels Token Handling* did with the pixels. When one column block has data from one of its pixels that needs to be read, it sets its *Hit* output high. The chip block detects this and starts the circulation of the token. As soon as one column block receives the token it will put its data (ADC data, row and column addresses) in the corresponding buses and send a request to the chip block. Once the chip block has read the data, it will set *Ack* high so that the token circulation can resume. The *Valid* signal is the same as *Req* and it is used to signal the external control and data acquisition system that data corresponding to a photon interaction is ready to be read. When a column block sets *Req* high it means that the data in the *Data*, *Row* and *Column* can be read.

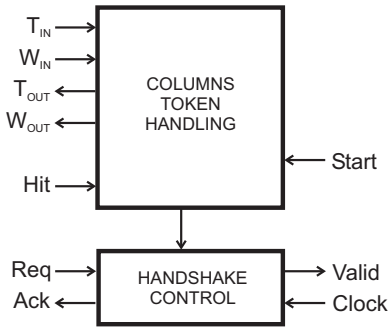

Figure 7.10: Block diagram of the chip control block.

7.2 Pixel data

So far, this chapter has shown the circuitry used in the pixels and in the periphery to select which pixel is being read, as well as the circuitry for reading the location in the array of the pixel. This section will explain the circuits used to read the digital data from the pixels. First, section 7.2.1 shows the circuit used to read the *done* and *row* signals explained earlier in section 7.1. Section 7.2.2 explains the circuitry used to read the ADC data from the pixel in the periphery of the readout chip.

7.2.1 Pixel control signals

The signals *done* and *row* are sent from the pixel to the column block in current-mode. This simplifies somewhat the pixel circuitry at the expense of complicating the receiver circuit.

The circuit shown in figure 7.11 converts these current-mode signals to a logic voltage level. Such a circuit is needed for each line (one for *done* and one for each bit of the *row* address).

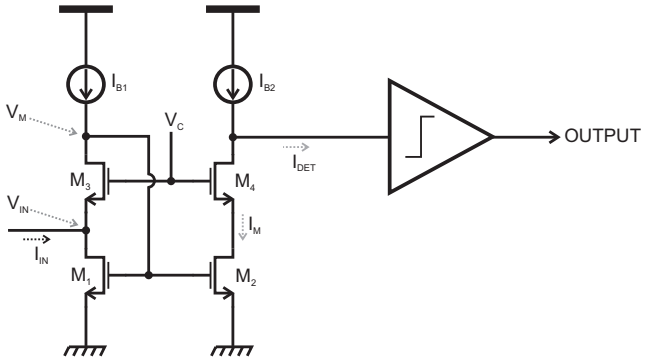

Figure 7.11: Implementation of the current detector circuit.

The node V_{IN} is connected to the column-long line corresponding to any of the signals mentioned earlier. The voltage swing at this node must be kept as close to zero as possible by keeping the input impedance of the circuit as low as possible. If this is accomplished the detection of the signal will be, to a first order approximation, independent of the capacitance of the line.

Transistors M_3 and M_4 are used as cascode transistors, while transistors M_1 and M_2 form a current mirror which copies the current entering the circuit (I_{IN}) in order to isolate the detection from the input node. Transistor M_3 isolates the gate from the drain of the diode-connected transistor M_1. This means that only the gate voltage (V_M) changes with the input current, while V_{IN} barely moves from its DC value or, in other words, the V_{GS} voltage of M_1 changes while its V_{DS} is kept (almost) constant. The two biasing currents I_{B1} and I_{B2} must have the same value. I_{B1} is used to bias transistor M_1 and equally I_{B2} biases M_2 so that:

$$I_{B1} + I_{IN} = I_M = I_{B2} + I_{DET} \tag{7.2}$$

If $I_{B1} = I_{B2}$ then I_{DET} is equal to I_{IN}.

The current comparator shown in figure 7.11 has been implemented in the pixADC4 prototype chip as the comparator explained in section 5.2.1. In the final implementation a small *threshold* current source must be added at the input of the comparator to compensate for current mismatches and to increase the noise immunity of the circuit. The output of the comparator is the digital signal that is used in the different logic circuits.

The original design was not thoroughly simulated prior to evaluation. In particular, a good approximation of the load at the V_{IN} node was not used in the simulations. This might have been one of the reasons for the failures during evaluation. Figure 7.12 shows the simulation results of the original circuit with a realistic estimation of the load. It's clear that the circuit suffers from instability. Modifications in the size of the bias transistors and in the voltages needed taking into account the real load can correct this problem, as the simulation in 7.13 shows

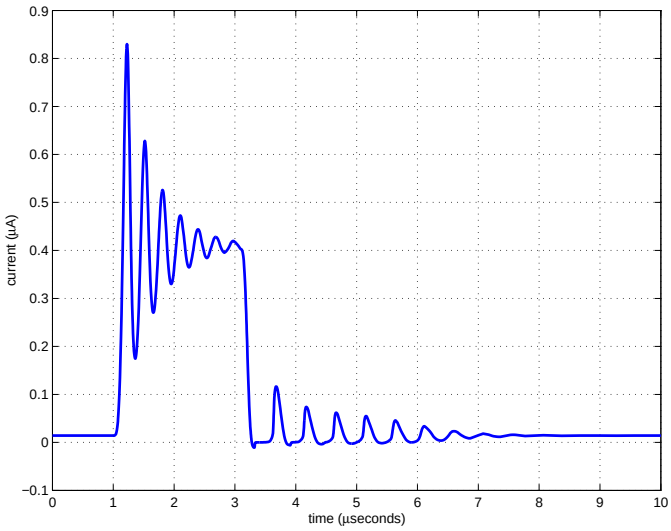

Figure 7.12: Simulation result under realistic load conditions of the original circuit.

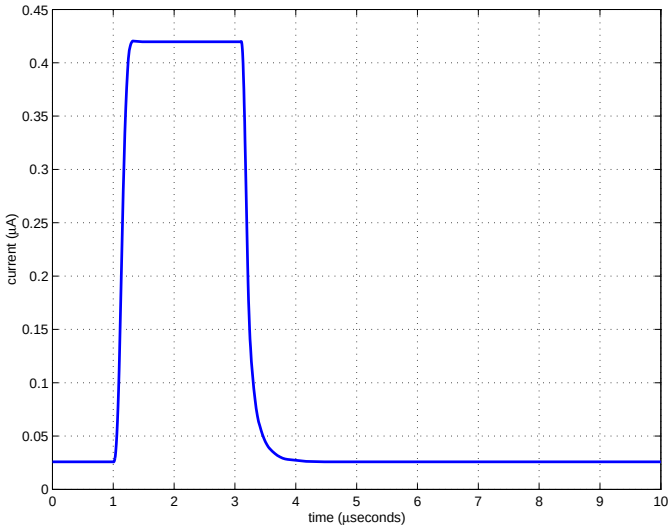

Figure 7.13: Simulation under realistic load conditions with modified biasing.

7.2.2 ADC data

Because of the array structure of the pixels and the digital nature of the data to be read, each pixel is treated as a SRAM cell with four bits of information. This allows the use of known circuitry for the storage and readout of the digital data.

Figure 7.14 shows the schematic of one of the flip flops used in the register of the successive approximation (figure 6.5) or algorithmic ADCs (figure 6.12). In both cases, the second latch in the flip-flop is modified to work like a conventional four transistor SRAM cell[2] by adding two switches.

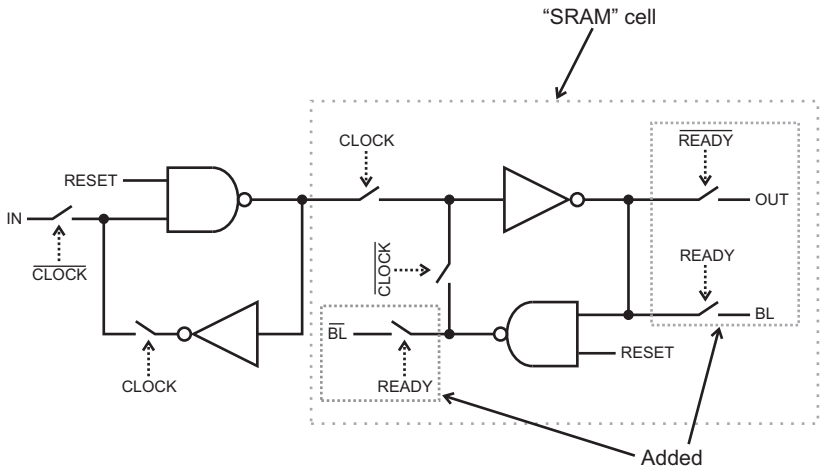

Figure 7.14: A common D flip flop modified for SRAM operation.

The *clock* signal in the figure is the clock input to the flip-flop (i.e. the decoder output in the successive approximation ADC as shown in figure C.6 or the *latch* signal in the algorithmic as shown in figure 6.13.). *Out* is the conventional voltage output of the flip-flop. BL and $overline BL$ are the two data outputs that will be read by the sense circuitry explained later in this section. There is one such pair of signals for each bit of data in the pixel ADC. The *ready* signal connects the memory element to the column-wide data bus, and it is generated in the circuit shown in figure 7.15.

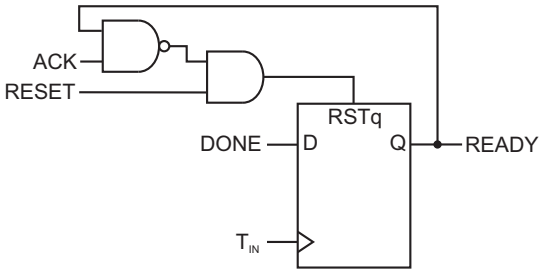

Figure 7.15: Generation of the READY signal in the pixel.

Figure 7.16 shows the schematic drawing of a typical SRAM cell, which corresponds to the equivalent circuit of figure 7.14 when *clock* is low and *reset* is high.

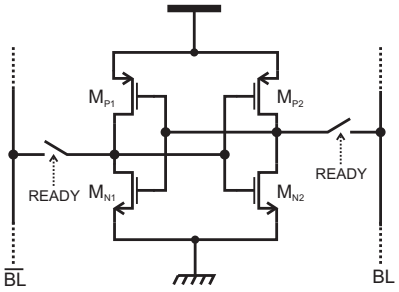

Figure 7.16: Schematic drawing of a typical SRAM cell.

When *ready* is high, the two complementary outputs of the SRAM cell are connected to the two column-long differential bit lines BL and $\overline{BL}$. To read these two values, a sense amplifier such as the one shown in figure 7.17 is typically used [2].

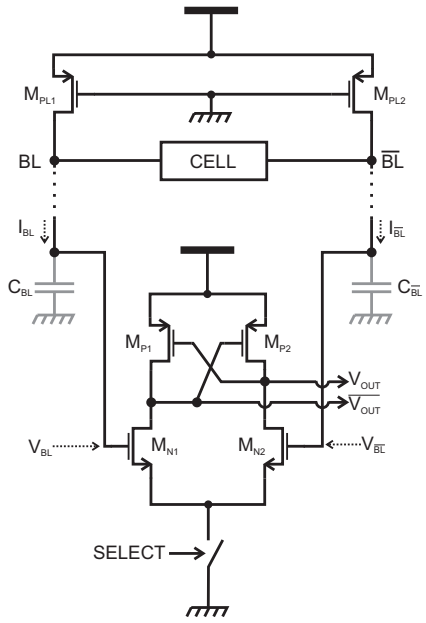

Figure 7.17: A typical implementation of a voltage-mode sense amplifier.

A small differential voltage is generated in the bit lines by the selected SRAM cell (pixel). This differential voltage is the input to a voltage comparator. One side of the differential input will tend to go closer to the positive supply, while the other will tend to the negative supply. The capacitance of the bit lines and the W/L ratio of the transistors in the SRAM cell will influence the speed at which these lines are charged by the memory cells, and hence the speed at which the comparator settles to a logic output value (i.e. '0' or '1').

To make the sensing circuitry as independent of the capacitance of the bit lines as possible, our system uses current sensing. The voltage in the bit lines is kept almost constant, and a circuit with a low-ohmic input impedance detects the current being sent from the memory cells [3, 4]. The implemented circuit is shown in figure 7.18.

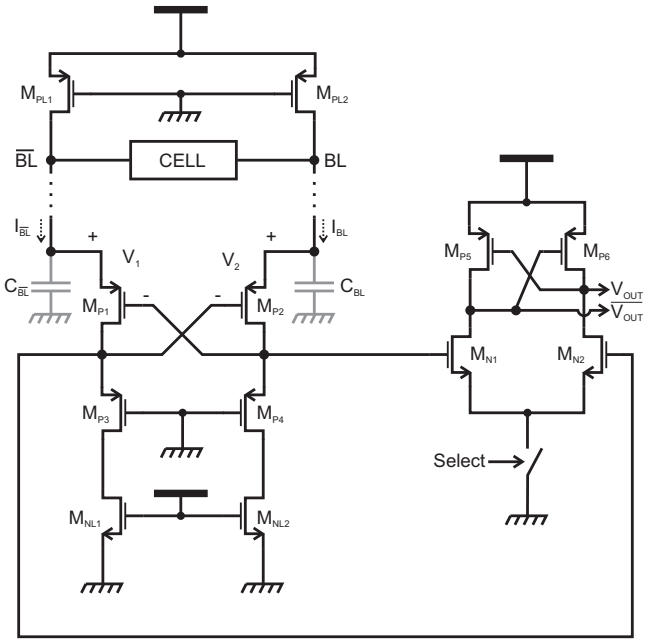

Figure 7.18: A possible implementation of a current-mode sense amplifier.

7.3 Experimental results

The circuits explained in this chapter were implemented in the pixADC4 prototype chip. The design was first checked by writing Verilog models of all the circuits and simulating them in different conditions. After the design was verified in Verilog, the transistor implementation of the different blocks was checked. All the digital circuits work with a supply voltage of 1 V.

Figure 7.19 shows the setup used to measure the pixADC4 prototype chip. Figure 7.20 shows the input *Test* signal (in red) and the resulting token (in blue) measured at the output of the chip block. Figure 7.21 shows again the token measured at the output of the chip block (in blue) as well as the signal indicating that the token circulation has ended (in red).

The complete system could not be verified due to errors in the readout of the pixel control signals.

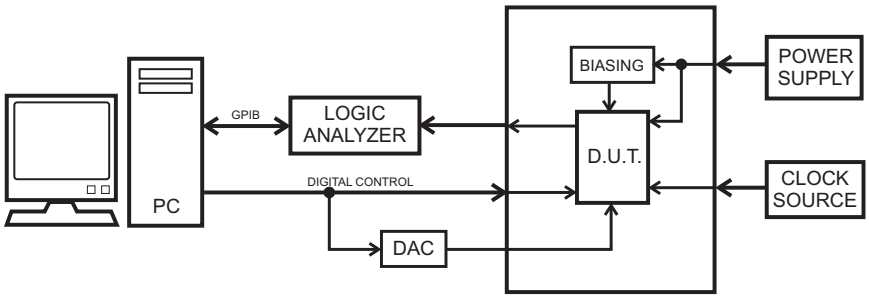

Figure 7.19: Set-up for the measurements of the array of ADCs in the pixADC4 prototype chip.

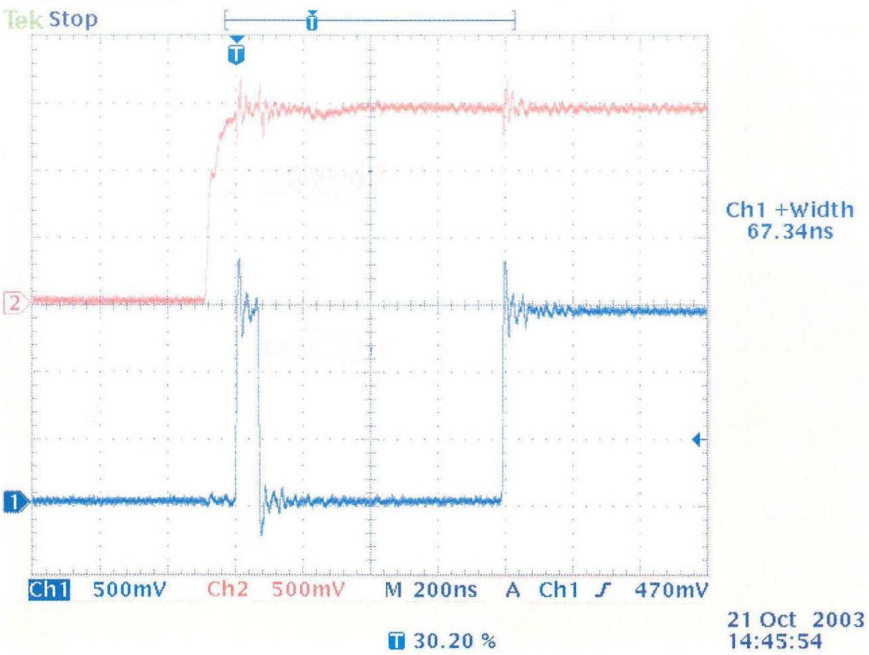

Figure 7.20: Test input (red) and measured token signal (blue).

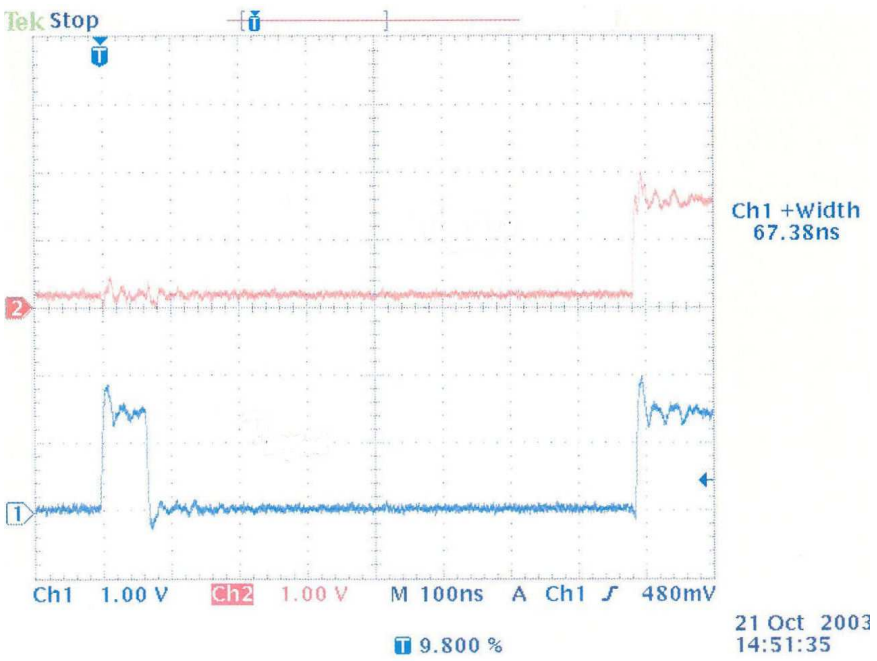

Figure 7.21: Measured token signal (blue) and token-circulation-finished (red).

7.4 Summary and conclusions

In order to read the location of the pixel hit by a photon as well as the result of the ADC conversion, a token passing architecture is used. A *token* circulates through the pixels. When a pixel which has processed a photon interaction receives the token, it takes control of a bus where it puts its address in the pixel array as well as the contents of the ADC. The pixels are organized in groups of two columns, and each two-column group has a control and readout block. The column control and readout blocks control the circulation of the token in their columns and read the data from the pixels. The same token passing architecture is implemented for these column control blocks.

Signals are sent from the pixels to the readout blocks in current mode to simplify the design of the pixels. For the same reason, signals being sent to the pixels from the periphery are sent in voltage-mode.

Bibliography

[1] I.E. Sutherland. Micropipelines. *Communications of the ACM*, 32(6):720–738, June 1989.

[2] N.H.E. Weste and K. Eshraghian. *Principles of CMOS VLSI design: A systems perspective*. Addison Wesley, 1994.

[3] E. Seevinck et al. Current-Mode Techniques for High-Speed VLSI Circuits with Sense Amplifier Application to Current for CMOS SRAMs. *IEEE Journal of Solid-State Circuits*, 26(4):525–536, April 1991.

[4] N. Shibata. Current sense amplifiers for low-voltage memories. *IEICE Transactions on Electronics*, E79-C(8):1120–1130, August 1996.

Chapter 8

Final conclusions

Continuous advances in semiconductor technology lead to the integration of more and more signal processing power into smaller areas. Additionally, advances in packaging technologies allow the interconnection of specialized sensors to conventional (CMOS) readout electronics, for example in hybrid imaging detectors. All these technological advances can be put to use in the field of X-ray imaging to allow a more efficient use of the information carried by the photons, such as their energy or the time of their arrival.

This thesis describes a CMOS readout chip for *spectroscopic quantum imaging* with hybrid pixel detectors. The system is composed of the sensor, usually manufactured in a semiconductor material, and the readout chip. Each photon absorbed by the sensor deposits an amount of charge proportional to its energy. This charge is read and processed by the readout chip. The resulting data is then transmitted off chip for further processing, storage or display. To obtain detailed images, both the sensor and the readout chip are subdivided into small pixels, and each pixel in the sensor is electrically connected to a pixel in the readout chip. A spectroscopic quantum imaging system measures the charge deposited in each pixel by each individual photon. Taking all this into account, this system could also be called a *color X-ray camera*.

Processing and transmitting the signals in the digital domain is the best option in such a complex system. To accomplish this, the charge deposited by the photon must be converted from an analog to a digital value as soon as possible. This means that analog-to-digital converters must be placed early in the signal processing chain. The ultimate option is to have an analog-to-digital converter in each pixel of the readout chip. These analog-to-digital converters must obviously very small and consume very low power. If this is achieved, one can even think of performing digital signal processing in the pixels themselves, possibly lowering the overall data rate and simplifying the overall system.

In this work we looked at two different ADC architectures in order to find the most suitable: successive approximation and algorithmic. The most efficient architecture turned out to be the successive approximation. Chapter 4 describes the complete readout chip, while Chapter 5 explains the pre-processing needed before the ADC. The two ADCs are described in Chapter 6.

The biggest challenge of the system is not so much the design of the pixel-ADCs, but how to transfer all the data from the pixels. The photons arrive asynchronously to the sensor, and the photon rate depends both on the source

and on the object being imaged. This means that the photon rate can be very different from pixel to pixel. In order to handle this, the readout chip should work in an asynchronous manner. This means that once a pixel is hit by a photon and the charge deposited in the sensor has been converted to a digital value, it should send its data off chip, e.g. to a data processing and display subsystem. The system described in this thesis uses such an asynchronous, data-driven architecture, as explained in Chapter 7.

This thesis described first the electronics which process the charge deposited by the photon before the analog-to-digital conversion. The circuits used are well known in the field and are very similar to the circuits used in the Medipix2 readout chip. The only novelty here is the use of different supply voltage domains for the analog signal processing (the charge sensitive amplifier and the peak-and-hold circuit) and for the hit detection circuits. The output of the hit detection circuit is a digital signal which will be used in the digital portion of the ADC as well as in the digital readout circuit. This allows us to use a lower supply voltage both in the hit detection circuit and in all other digital circuits, in order to lower the power consumed in the pixels.

The use of pixel-level ADCs in a quantum imaging system is the first new thing introduced in this thesis. These ADCs must be located in each pixel of the readout chip. These ADCs function independently of one another. The second new thing is the asynchronous, event-driven readout architecture of the pixels in the imaging array. Each photon interaction is processed and read from the pixel independently, and the readout sequence is started by the pixels.

The work described in this thesis shows that complex signal processing at the pixel level is possible in quantum imaging systems based on hybrid pixel detectors. Nevertheless, the system described in this thesis could be extended while keeping the same architecture. For example, by adding information on the time the photon hit the pixel. Or by adding more digital processing in the pixels to, for example, account for photons hitting more than one pixel at the same time.

The recent development of chips like the TimePix[1] and the CIX[2] show a trend towards quantum spectral imaging using photon counting as a starting point, further validating the ideas explained in this thesis.

Bibliography

[1] X. Llopart et al. Timepix, a 65k quantum imager readout chip for arrival time, energy and/or event counting measurements. In *2007 International Image Sensor Workshop*.

[2] H. Krueger et al. CIX: a detector for spectrally enhanced x-ray imaging by simultaneous counting and integrating. In *SPIE 2008 Medical Imaging Conference*.

Appendix A

Bias distribution

Some of the circuits located in the pixels, such as current sources and cascode transistors, need to be biased in order to operate correctly. The reference bias values can be generated in the chip itself or applied externally. Generating the bias values in the chip, for example using on-chip digital-to-analog converters (DACs), simplifies the overall system design, especially when more than one pixel readout chip must be used for large area coverage.

In the following it is assumed that the bias values in the system are generated by dedicated on-chip DACs. It will not be discussed how these DACs are programmed or how the DAC reference value is generated, as these issues are very dependant on the complete system implementation. In [1] the design of on-chip DACs to generate the bias values for two pixel detector readout chips is explained in detail more.

The distribution of the bias values must be performed in a way such that the performance of the pixels across the chip is as uniform as possible. This does not mean that the bias values must be equal across the chip, but rather that the locally applied bias (i.e. at the pixel level) must follow the differences in the threshold voltage of the transistors in the chip. These differences can be a result of inherent fabrication issues, temperature differences or radiation damage. An additional effect that must be carefully evaluated is the voltage drop in the supply and bias distribution lines from the periphery to the pixels, as well as across the pixels. These voltage drops are due to the resistance of the metal wires used to distribute the power supply and the bias values. These two considerations point to a bias distribution scheme where the bias values are sent as currents to the pixels and reproduced locally via a diode-connected transistor (i.e. by current mirrors).

A.1 Distribution of bias currents

Figure A.1 shows the most effective way, in terms of uniformity, to distribute bias currents to the pixels *.

*In all the figures following it is assumed that a reference voltage generated e.g. by an on-chip bandgap reference is used to bias the DACs. The origin of this value, as well as the design of the reference circuit has no influence on the discussion in this section.

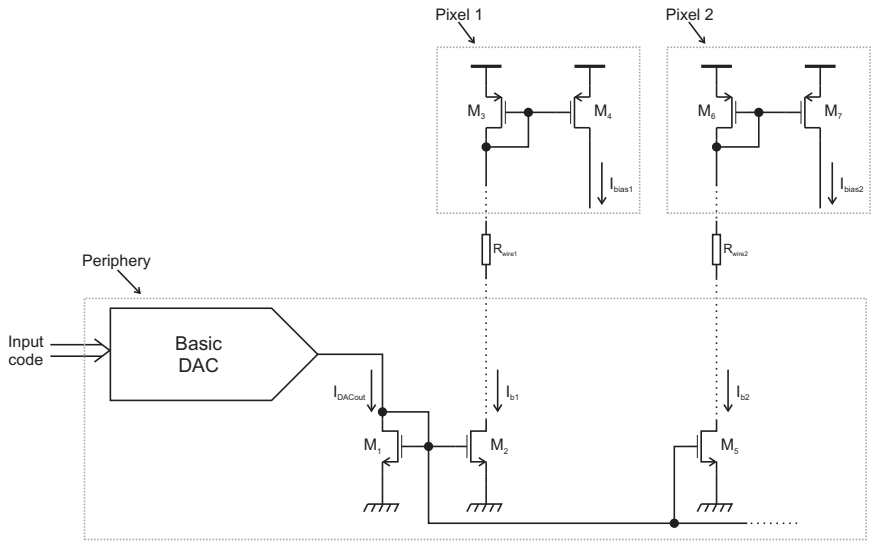

Figure A.1: Current copying from the DACs to the target transistor using one dedicated connection for each target transistor.

In this implementation the output of a current-steering DAC (I_{DACout}) is mirrored by the matched transistor pairs M_1-M_2, M_1-M_5, etc. for each pixel in the imaging array. This mirroring stage can eventually be also used to scale the DAC output current to the appropriate values needed for I_{b1}, I_{b2}, etc. These currents are then sent to the pixels, where another current mirror is used to generate the appropriate gate-source voltage needed by the transistors M_4, M_7, etc. to operate as current sources, or to use the gate-source voltage to bias a cascode transistor.

The figure does not show the wiring resistances in the reference positive and negative supply values between the periphery and the chips and between the chips themselves. The values of these resistances as well as the resulting differences in supply references are strongly dependant on the chip layout. By effectively sending a current from the periphery to each pixel, all voltage mismatches between pixels and between pixels and periphery have no (or a minimal) influence on the final value. For the same reason, variations in the threshold voltage of the transistors (e.g. due to radiation damage) between the pixels or between the periphery and the pixels will have no detrimental effect either. Due to the relatively low values of the bias currents needed, voltage drops in the lines carrying the current from the periphery to the pixels (I_{b1} and I_{b2} in the figure) due to the wiring resistances (e.g. R_{wire1} and R_{wire2} in the figure) should be negligible if correct circuit layout techniques are used. The only source of inaccuracies is the quality of the matching of the transistors used in the current mirrors in the pixels ($M_3 - M_4$ and $M_6 - M_7$ in the figure) and in the periphery ($M_1 - M_2$ and $M_1 - M_5$).

This method of distributing the bias currents to the pixels has two very important drawbacks. First, it needs an extremely large number of interconnect lines between the DACs in the periphery and the pixels. And second, the static power consumption is relatively large (effectively doubled) because the total

bias current needed is used twice: once in the periphery and once in the pixel (e.g. I_{b1} and I_{bias1}).

Figure A.2 shows a second possibility for distributing the bias currents to the pixels which eliminates the problem of the large number of interconnects by connecting all the pixels to one DAC via a single interconnect line.

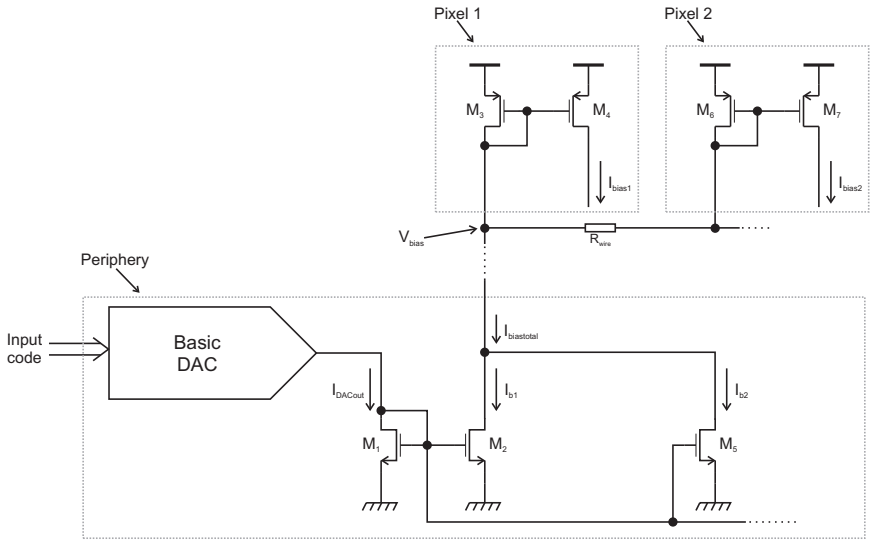

Figure A.2: Current copying from the DACs to the target transistor using one interconnect for each bias value.

As in the scheme presented in figure A.1, the output of the DAC (I_{DACout})is mirrored once for each pixel by the current mirrors $M_1 - M_2$, $M_1 - M_5$, etc. In this case, however, the outputs of all the mirrors (the drains of transistors M_2, M_5, etc.) are connected together and this added current is then distributed to all pixels.

This time, mismatches in threshold voltage between the transistors in the pixels and differences in the value of the power supply values from pixel to pixel will have an influence on the value of the bias current used in the pixel. Also, the wiring resistance R_{wire} connecting all pixels will also change the effective V_{bias} seen by the different pixels. All this will result in different local bias currents.

A.2 Distribution of bias voltages

To minimize the size of the pixels and the static power consumption, most pixel detectors used for radiation detection do not use either of the methods described earlier to distribute the bias currents, but the method shown in figure A.3.

Instead of copying the current from the DAC to the pixels, the *gate voltage* needed in the pixel to bias the transistor as a current source or cascode transistor is copied from the periphery to the transistors in the pixels. By not using a current mirror in each pixel, smaller pixel sizes can be achieved, specially since the transistors used as current sources tend to be relatively large. Additionally,

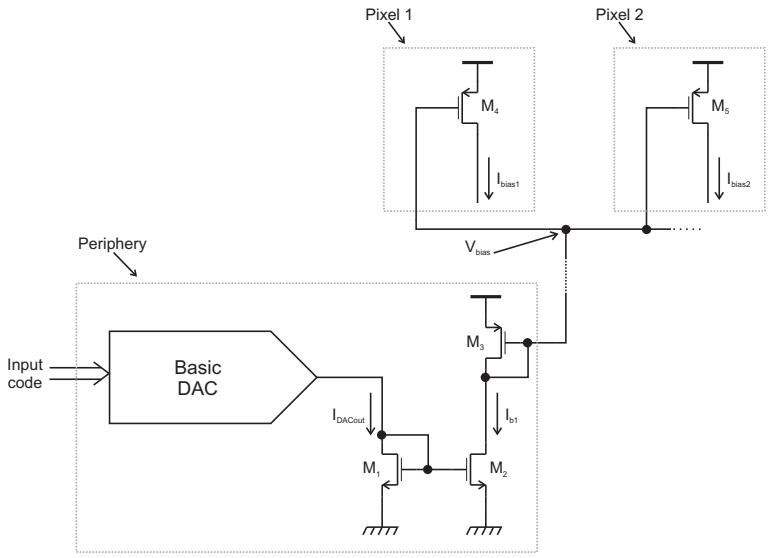

Figure A.3: Current copying from the DACs to the target transistor by distributing the gate voltage.

the static current consumed by the chip diminishes with respect to the methods described in section A.1 because the bias currents are only used once in each pixel. Note also that there is no current flowing through the interconnection between the periphery and the pixels.

This method, however is not as good for uniform bias distribution as the ones shown in figures A.1 and A.2. The transistor pairs M_3-M_4 and M_3-M_5 cannot be considered as matched pairs anymore as the transistors are located far away from each other. Also, the current generated in each pixel depends on the value of the transistor's threshold voltage and the value of the supply voltage values in the pixel. Differences in these values between the transistors in the different pixels and between the periphery and the pixels will translate into differences in the current generated locally in the pixels. These differences in threshold voltage between pixels are intrinsic to the fabrication of the devices and can be exacerbated by radiation damage.

This method is also used to distribute *pure* voltage references, such as the reference input in a pseudo-differential stage or in a comparator. In this case the biggest obstacle for a correct distribution of the value to all pixels will be the differences in the voltage drop in the supply lines. The value used locally in the pixel is the voltage sent from the periphery referenced to the local positive or negative supply value, but the local supply values in each pixel will be different from pixel to pixel and between the periphery and the pixels.

A method to compensate for the effects of voltage drops in the supply lines has been used in the last version of the readout chip for the ATLAS pixel detector [2]. This method involves copying not only the *reference voltage*, but also the *reference supply voltage* from the periphery to the pixel array. It is not needed to implement this bias compensation in all pixels, as pixel to pixel drops within a certain distance can be considered negligible.

Bibliography

[1] D. San Segundo Bello. Design of the bias DACs for the ALICE/LHCb and Medipix2 pixel readout chips. Internal report.

[2] L. Blanquart. FEI-2: A Front-End Readout Chip designed in a commercial 0.25μm process for the ATLAS Pixel Detector at LHC. In *Proceedings of the IEEE Nuclear Science Symposium and Medical Imaging Conference, Portland, October 19-25, 2003.*

Appendix B

Design for test

This appendix describes an approach to include test capabilities in the design of the system. The basic idea is to check the different functional blocks for functionality and performance. This allows selecting the best dies before the full system is built as the process of connecting the electronics chip to the sensor is typically one of the most expensive steps in the manufacturing of the imaging system. It also allows a characterization of parts of the system for later off-line correction and/or calibration.

The blocks that need to be tested are the biasing and the off-chip communication blocks in the periphery and the front-end and ADC circuits in the pixels.

The process to test the readout electronics chip would follow these steps. First, the communication blocks are verified by sending data to the chip and then reading data from the chip. Next, the biasing circuitry can be verified by programming the bias DACs and measuring their outputs using dedicated circuitry. The configuration bits for the pixels should also be verified, e.g. by writing to the configuration registers in the pixels and reading the data back. Next, the token circulation must be also verified as described in section B.1. Once the functionality of the token circulation and biasing has been correctly verified, the characteristics of the pixel ADCs can be measured as explained in section B.2. Finally, with the ADCs characterized, the pixel front-end electronics can also be verified as section B.3 explains.

B.1 Token circulation

To test the token passing between the column blocks, the *Done* input to the *Columns token handling* circuitry of the chip block shown in figure 7.10 can be overridden by a *Test* signal. The time can be measured between the rising edge in the *Start* signal and the rising edge of the token arriving from the last column block (T_{IN} input).

A second test, similar to the first one, can be performed for every group of pixels belonging to a column block. This test can be done one column block at a time or for all columns in parallel.

Finally, the circuitry used to sense the data from the pixels can be tested by using the *pixel configuration block* shown in igure 4.3. A known bit pattern

of bits can be written into the pixels and a test mode can be implemented in the pixel readout block that overrides the *Hit* signal. All pixels from the two columns will be read in sequence. When the two columns have been read, the test mode in the pixels is turned off and the read data is compared to the written pattern.

B.2 Analog to digital converter DFT

The purpose of the ADC design-for-test circuitry is to be able to characterize all the ADCs in the array. Due to the nature of the signal being converted only the static input/output characteristics of the ADC must be checked. Once this data is available it can be used to disable pixels which show a very bad performance or for off-line calibration of the ADC output data. One important issue in this process is that the ADC characterization must be done (in principle) independently of the front-end electronics.

In [1] two ways to realize a BIST (built-in self-test) system for testing and characterizing an array of ADCs were investigated. The BIST system is designed to indicate that the linearity of the ADCs fulfills some specification entered externally or hardwired in the chip. But it can be easily modified to record the full transfer characteristic of each ADC for off-line calibration. figure B.1 shows the basic idea behind both methods.

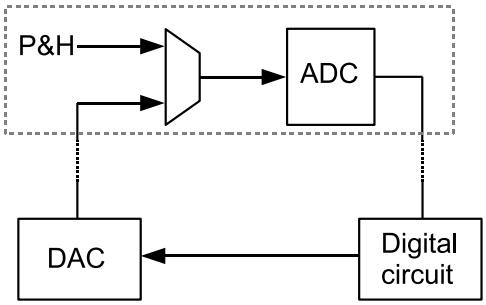

Figure B.1: Basic idea of the built-in self test circuitry for an array of ADCs.

A DAC with a resolution higher than the resolution of the pixel ADCs and with very good linearity is used. The output of this DAC is applied to each ADC in turn and the digital output of the ADC is analyzed to measure its static linearity (INL and DNL). Apart from the DAC, only some simple digital circuitry to measure the linearity of the ADC is needed in the peripheral electronics. The pixel electronics must be slightly modified to allow for this test. A couple of switches must be added to the input of the ADCs in the pixel to select the DAC output as the input to the ADC instead of the output of the peak-and-hold circuit.

The system described in [1] uses direct addressing to select the pixels. In order to use the token-passing architecture used in our system, the following steps should be followed. First, an additional test signal is added to the two-column block signals. Also, a specific bit in the pixel configuration register must

also be reserved. This bit will be activated for all pixels which will be tested before starting the test.

The token circulation starts in the usual way. When the token arrives to a pixel which had its test bit activated, the pixel behaves as if it had a photon hit processed and data ready to be read out and it sets *DONE* high. The column block sees this and sets the column-wide *TEST* signal high. At this point the test circuit starts sweeping the DAC codes. The column block will set *ACK* high whenever a new DAC value is ready. When the conversion is finished, the pixel will set *REQ* high and the test circuit will react by putting a new value in the DAC. When all DAC codes have been measured, the column blocks sets the *Test* signal low. The pixel which was being tested sees this and lets the token pass.

B.3 Front-end electronics

For the front-end electronics, the behavior of the integrator, hit detector and peak-and-hold must be evaluated for different values of input charge. To generate the input charge electronically (i.e. without being connected to a sensor), the circuit shown in figure B.2 can be used.

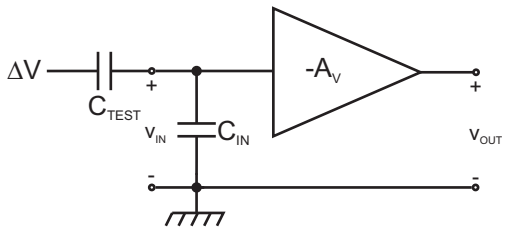

Figure B.2: Basic configuration for testing electrically the front-end electronics.

Applying a controlled voltage step to one of the plates of the C_{TEST} capacitor, a known value of charge will be injected into the amplifier. If C_{IN} is the equivalent input capacitance as calculated in Equation 5.3, the charge injected into the amplifier is:

$$Q_{TEST} = \Delta V \cdot C_{TEST} \cdot \frac{C_{IN}}{C_{IN} + C_{TEST}} \tag{B.1}$$

If C_{IN} is much larger than the test capacitance (C_{TEST}), then the charge injected into the amplifier can be calculated as:

$$Q_{TEST} = \Delta V \cdot C_{TEST} \tag{B.2}$$

The combined performance of the input amplifier and hit detector can be characterized by scanning the global threshold values and looking at the hit signal.

The combined performance of the input amplifier and peak and hold can be done once the ADC has been characterized as explained in the previous section.

Bibliography

[1] D. San Segundo Bello and E. Wolthuis. A BIST system for an array of static analog-to-digital converters. Technical report, University of Twente, 2000. Available at: http://www.nikhef.nl/user/dbello/reportbist.pdf.

Appendix C

Digital circuits

This appendix shows the schematics of some of the digital circuits used in the design but not explained in the preceding chapters. The digital circuits used in the successive approximation ADC are shown in section C.1. Section C.2 shows the circuits used in the readout blocks explained in chapter 7.

C.1 Successive Approximation Analog-to-Digital Converter

As shown earlier in section 6.3, the successive approximation ADC has a relatively large amount of digital circuitry. Figure C.1 shows again the block diagram of the digital circuitry in the ADC.

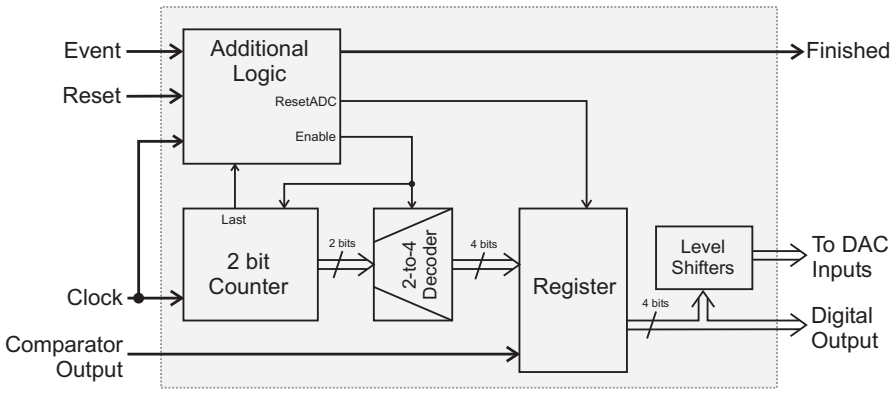

Figure C.1: Block diagram of the digital control for the successive approximation ADC.

This section will show the schematics of the different blocks: the counter, the decoder, the register and the additional logic.

A gate-level schematic of the counter is shown in figure C.2, and the decoder is shown in figure C.3.

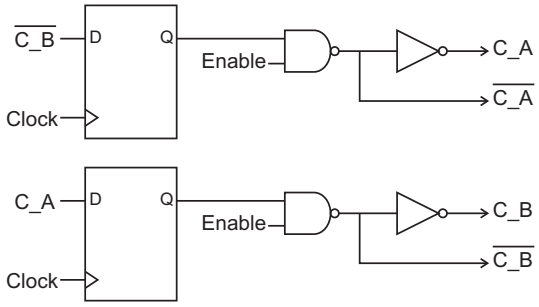

Figure C.2: Schematic of the counter.

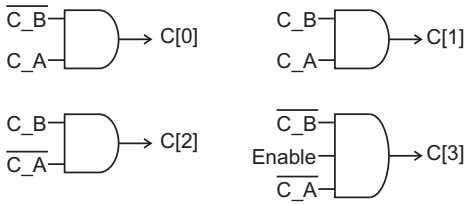

Figure C.3: Schematic of the decoder.

Figure C.4 shows the implementation of the *additional logic* block. The $C[0]$ input signal corresponds to the output of the counter indicating the last state as shown in figure C.3.

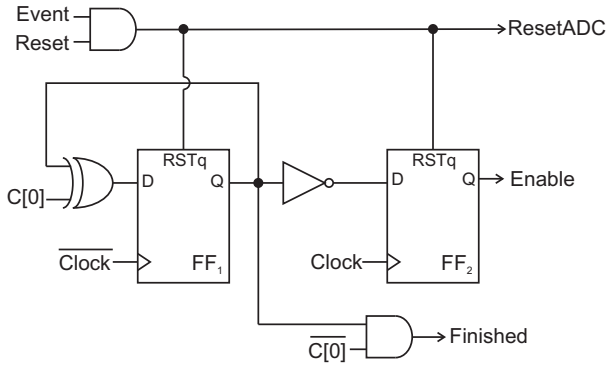

Figure C.4: Schematic of the additional logic block.

A explanation of this additional logic block follows. While *Reset* or *Event* are low, the outputs of the two flip-flops as well as *ResetADC* are set low*. As long as the output of the flip flop FF_1 remains low, *Finished* will also be low.

*The reset signal in the flip-flops is active low.

The signal $C[0]$ will also be low, as the counter will be disabled (*Enable* is low). At the first rising edge of the clock after *Reset* and *Event* are both high, *Enable* will go high and the counter will start to count. When the counter arrives to its last state, both $C[0]$ and the output of the XOR gate go high. At the next falling edge of the clock the output of the flip-flop FF_1 goes high and the output of the XOR goes low. The next rising edge of the clock will set $C[0]$ low, the output of flip-flop FF_2 (*Enable*) will go low disabling the counter and *Finished* will go high until either *Event* or *Reset* go low. Figure C.5 clarifies the function of this block with a timing diagram.

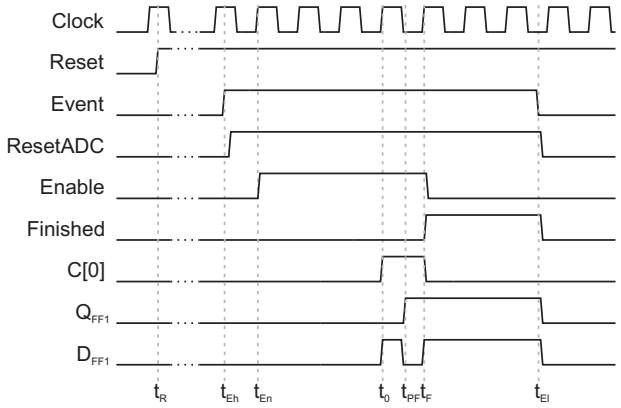

Figure C.5: Timing diagram showing the functionality of the additional logic block.

Figure C.6 shows the implementation of the circuitry corresponding to each bit in the register.

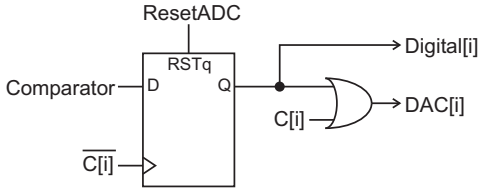

Figure C.6: Schematic of one bit of the register.

For each bit there are two outputs. One of them is applied to the DAC ($DAC[i]$), and the other is the actual digital output of the ADC corresponding to bit i ($Digital[i]$). When the counter signal corresponding to this bit ($C[i]$) is high, $DAC[i]$ must be high. At the moment that $C[i]$ goes low, the output of the comparator is sampled. If the input to the ADC is smaller than the output of the DAC, the output of the comparator will be low, bit $DAC[i]$ will go low and the digital output will also stay low. If the analog input is larger than the output of the DAC, the output of the comparator will be high, bit $DAC[i]$ must

remain high and the digital output corresponding to bit i must also go high.

C.2 Readout

The different digital circuits corresponding to the readout functional blocks are shown here with more detail. First, the C element is explained in section C.2.1. Next, the pixel handling block is shown in section C.2.2. The *REQ* detector is explained in section C.2.3. Section C.2.4 explains the remaining pixel and column logic. Finally, section C.2.5 explains the column token handling.

C.2.1 C element

This logic gate is a fundamental building block in digital asynchronous logic circuits. Figure C.7 shows the transistor implementation of a static C element with reset*.

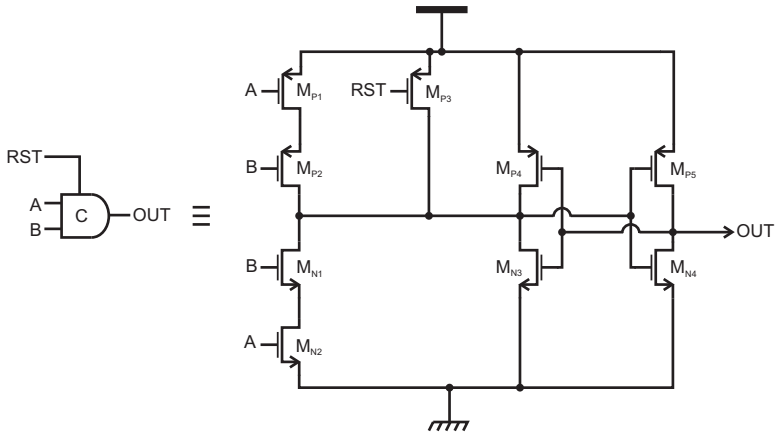

Figure C.7: Transistor implementation of a C element.

The reset input *RST* is used to set the output of the C element to a known value in absence of input excitation. When *RST* is low, the output of the C element is set low. When *RST* is high, the output of the C element will follow its two inputs as follows. If both A and B are low, the pMOS transistors M_{P1} and M_{P2} are turned ON and the output of the C element is set low. If both A and B are high, transistors M_{N1} and M_{N2} are turned ON and the output of the C element is set high. If A and B have different values, the output of the C element will keep its last output value (either the last value when both inputs were equal or the value after a reset). The last output value is stored in the internal node of the C element by the pair of cross-coupled CMOS inverters formed by transistors M_{P4}, M_{P5}, M_{N3} and M_{N4}.

*The term *static* refers to how the internal state of the C element is stored. In a *static C element* a static memory cell (two cross-coupled inverters) is used. A *dynamic C element* uses only an internal capacitance to store the internal state.

C.2.2 Pixel handling block

Figure C.8 shows the implementation of the pixel handling block circuit. This circuit starts the circulation of the token in a two-column block.

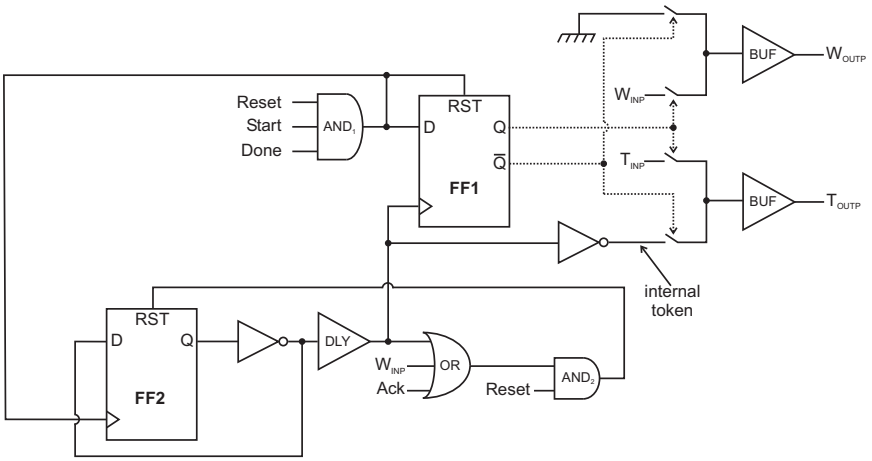

Figure C.8: Implementation of the pixel handling block.

The circuit can work in two modes: if the first pixel in the token ring has data to be read (W_{INP} is high) or not (W_{INP} is low). Figure C.9 shows a basic timing for the second case.

If *RESET* is low the two flip flops are reset, W_{OUTP} is set low (connected to ground) and T_{OUTP} is connected to the *internal token* signal. Because the $FF2$ flip-flop is reset, the internal token signal is low and at least one input to the OR_1 gate is high, making the output of the gate also high. When *RESET* goes high, the two inputs to AND_2 will be high and so the *RST* input of $FF2$ will also go high, enabling it. At the moment that *RESET*, *DONE* and *START* are high, the output of AND_1 will go from low to high. $FF2$ will see a rising edge at its clock input and will set its output high. After the delay time introduced by the *DLY* element*, one input to OR_1 will be low. The output of the OR_1 gate will then be low when the other two inputs (W_{INP} and ACK) are also low. This will happen when the first pixel in the first column has not processed a photon interaction (W_{INP} low) and when the ACK from the chip block is also low. At this point $FF2$ will be reset because the output of AND_2 will be low and consequently its output will be set low. $FF1$ will see a rising edge at its clock input after the delay time and the switches will connect T_{INP} to T_{OUTP} and W_{INP} to W_{OUTP}. At this moment the pixels in the two columns are organized in a closed ring until either *Done*, *Reset* or *Start* goes low. The default width of the token signal going to the first pixel of the first column will be equal to the value of the delay. However, if the pixel had processed a photon interaction before the token arrives, W_{INP} will be high, and the start-up circuit will have to wait to set the token low again as in the case shown in figure 7.5.

*This delay can be implemented as a chain of inverters or as a current starved inverter. In the pixADC4 prototype chip the last possibility was implemented.

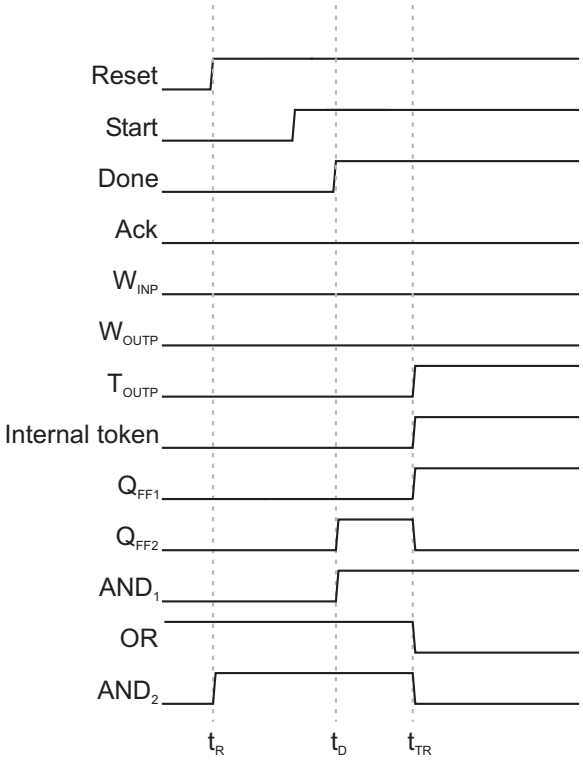

Figure C.9: Basic timing diagram of the pixel handling block.

C.2.3 REQ detector

Figure C.10 shows the implementation of the circuitry that reads the request signals from the pixels (Req_0 and Req_1) in the two columns.

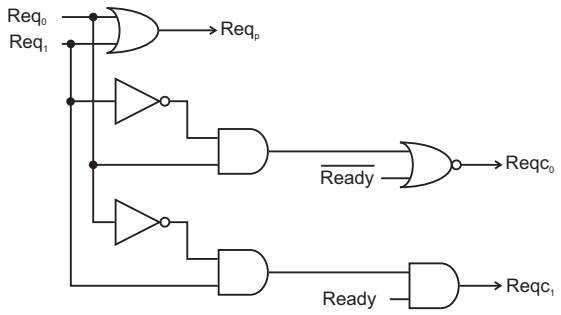

Figure C.10: Circuitry used to detect the Req signals from the pixels, and to generate the column address.

The *Ready* signal is generated in the same way as for the pixels (see figure 7.15), but using *State* instead of *Done*.

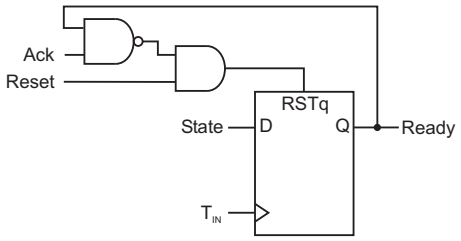

Figure C.11: Circuitry used to detect the Ready signals from the columns.

C.2.4 Other logic

The signal *State* is generated by the circuit shown in figure C.12.

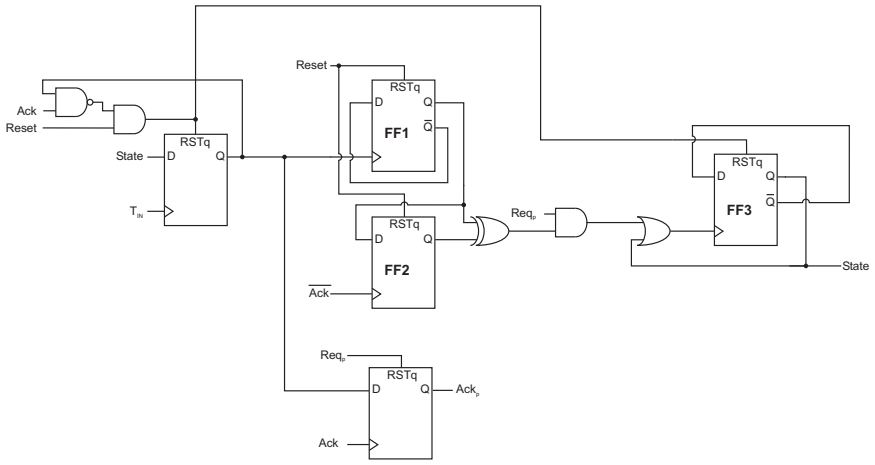

Figure C.12: Implementation of the circuit used to generate the State signal.

A short explanation of the circuit follows. After a reset the outputs of all the flip-flops are set low. The output of all the logic gates (XOR, AND and OR) are also zero. The output of flip-flop $FF3$ will go high only when Req_p and the output of the XOR gate are high and when the signal *State* is also high. The output of flip-flop $FF2$ will go high only when the output of the flip-flop $FF1$ is high and the signal *Ack* is low. The output of flip-flop $FF1$ will go high only when the signal *State* is high. The *Ready* signal will go high when *State* goes high. When *Ack* goes low, the output of $FF2$ and the output of the XOR gate go high. When Req_p goes high, the output of the AND and OR gates go high and the signal *State* goes high. When *Ready* goes high, the output of the XOR gate goes low and the output of the AND gate goes also low.

C.2.5 Column token circuitry

The token passing circuitry in the columns is implemented in a similar way as in the pixels, as figure C.13 shows.

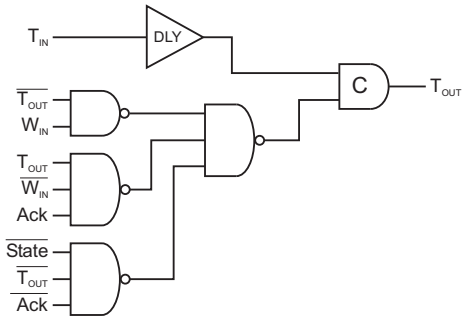

Figure C.13: Implementation of the token passing circuitry in the column block. Note that the reset input of the C element is not drawn.

List of publications

1. M. Burns, M. Campbell, E. Cantatore, V. Cencelli, R. Dinapoli, F. Formenti, T. Grassi, E. Heijne, P. Jarron, K. Kloukinas, P. Lamanna, M. Morel, V. O'Shea, V. Quiquempoix, **D. San Segundo Bello**, W. Snoeys, K. Wyllie, *"A pixel readout chip for tracking at ALICE and particle identification at LHCb"*, Fifth Workshop on Electronics for LHC Experiments, Snowmass, Colorado, USA, 20 - 24 September 1999

2. R.Dinapoli, M.Campbell, E.Cantatore, V.Cencelli, E.Heijne, P.Jarron, P.Lamanna, V.O'Shea, V.Quiquempoix, **D. San Segundo Bello**, W.Snoeys, B.van Koningsveld, K.Wyllie, *"An analog front-end in standard 0.25 um CMOS for silicon pixel detectors in ALICE and LHCb"*, Sixth Workshop on Electronics for LHC Experiments Krakow, Poland, 11 - 15 September 2000

3. **D. San Segundo Bello**, B. Nauta, J. Visschers, *"Pixel-Level Analog-To-Digital Converters for Hybrid Pixel Detectors with energy sensitivity"*, IEEE Nuclear Science Symposium and Medical Imaging Conference, Lyon, France, October 15-20 2000

4. **D. San Segundo Bello**, B. Nauta, J. Visschers, *"Design of pixel-level ADCs for energy-sensitive hybrid pixel detectors"*, Proceedings of the 11th ProRISC workshop, Veldhoven, The Netherlands, November 30 - December 1, 2000, pp.489-493

5. R. Dinapoli, M. Campbell, E. Cantatore, V. Cencelli, E. Heijne, P. Jarron, P. Lamanna, V. O'Shea, V. Quiquempoix, **D. San Segundo Bello**, B. Van Knoningsveld, K. Wyllie, *"A front-end for silicon pixel detectors in ALICE and LHCb"*, 8th Pisa Meeting on Advanced Detectors, La Biodata Isola dElba, Italy, 21 May 2000. Published in Nuclear Instruments and Methods in Physics Research A, volume 461, issue 1-3 (1 April 2001), pp. 492-495

6. W.Snoeys, M.Campbell, E.Cantatore, V.Cencelli, R.Dinapoli, E.Heijne, P.Jarron, P.Lamanna, D.Minervini, V.O 'Shea, V.Quiquempoix, **D. San Segundo Bello**, B.Van Koningsveld, K.Wyllie, *"Pixel readout electronics development for the ALICE pixel vertex and LHCb RICH detector"*, International Workshop on Semiconductor Pixel Detectors for Particles and X-Rays (PIXEL 2000), Genoa, Italy, 5-8 June 2000. Published in Nuclear Instruments and Methods in Physics Research A, volume 465, issue 1 (1 June 2001), pp. 176-189

7. **D. San Segundo Bello**, B. Nauta, J. Visschers, *"Design of analog-to-digital converters for energy sensitive hybrid pixel detectors"*, Second International Workshop on Radiation Imaging Detectors, Freiburg i. Br., Germany, July 2-6 2000. Published in Nuclear Instruments and Methods in Physics Research A, volume 466, issue 1 (21 June 2001) , pp. 218-225

8. W. Snoeys, M. Burns, M. Campbell, E. Cantatore, V. Cencelli, R. Dinapoli, E. Heijne, P. Jarron, P. Lamanna, D. Minervini, M. Morel, V. O'Shea, V. Quiquempoix, **D. San Segundo Bello**, B. Van Knoningsveld, K. Wyllie, *"Pixel readout chips in deep submicron CMOS for ALICE and LHCb tolerant to 10 Mrad and beyond"*, 4th International Symposium on Development and Application of Semiconductor Tracking Detectors (4th Hiroshima STD Symposium), Hiroshima, Japan, March 22-25 2000. Published in Nuclear Instruments and Methods in Physics Research A, volume 466, issue 2 (1 July 2001) , pp. 366-375

9. **D. San Segundo Bello**, B. Nauta, J. Visschers, *"Towards a single-photon energy-sensitive pixel readout chip: pixel level ADCs and digital readout circuitry"*, Proceedings of the 13th ProRISC workshop, Veldhoven, the Netherlands, November 28 and 29, 2002, pp.444-448

10. X. Llopart, M. Campbell, R. Dinapoli, **D. San Segundo Bello**, and E. Pernigotti, *"Medipix2: a 64-k pixel readout chip with 55 micron square elements working in single photon counting mode"*. IEEE Transactions on Nuclear Science, vol. 49, no. 5, October 2002, pp. 2279-2283

11. **D. San Segundo Bello**, M. van Beuzekom, P. Jansweijer, H. Verkooijen and J. Visschers, *"An interface board for the control and data acquisition of the Medipix2 chip"*, Proceedings of the 4th International Workshop on Radiation Imaging Detectors, Amsterdam, the Netherlands, September 8-12, 2002. Published in Nuclear Instruments and Methods in Physics Research A, volume 509, pp. 164-170

Acknowledgements

The road to this moment has been long, and I would not have made it without the support and friendship of many people I found along the way.

First and foremost, my parents, without whom I would not have been able to start the journey.

My sister, for being her.

My promotors, Bram and Jan. And Erik, who started it all.

During my work at NIKHEF I had the pleasure of working together with an amazing bunch of people: Ruud, Martin, Hans, Peter, David, Alessandro and everyone from the ATLAS SCT and the electronics workshop.

The time I was at Twente would not have been the same without: Ronald, Arnoud, Sasa, Svetoslav, Vincent, Simon, Eric, Jan-Rutger, Henk and all the other students and researchers from "vloer drie".

Everyone I met at CERN: Michael, Xavi, Walter, Ken, Bettina, Lukas, Eugenio, Roberto, Kostas and all the people from the Medipix collaboration.

And everyone who during the following years pushed me to get over my "neurosis" and finish once and for all what I had started: Hubert, Susana, Enrique, José Luis, Patrick, and everyone else I worked with during those years.

About the author

David San Segundo Bello was born on the 21st of August 1972 in LHospitalet de Llobregat (Spain). He obtained the title of Ingeniero Técnico en Telecomunicaciones in 1995 at the Ramon Llull University. He went on to study Electronics Engineering at the Barcelona Autonomous University (Universitat Autònoma de Barcelona), where he graduated in 1997. He did his final year project as a Erasmus student at Twente University. He enlisted as a PhD student at NIKHEF in Amsterdam and Twente University in 1998. The results of that work are contained in this thesis. From 2004 until 2008 he worked as a mixed-signal designer for Infineon Technologies Austria in Villach (Austria). Since 2008 he is working at IMEC in Leuven (Belgium).